IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD.,

Plaintiff,

Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF)

٧.

CHI MEI OPTOELECTRONICS CORPORATION, et al.

Defendants.

CONSOLIDATED CASES

DECLARATION OF ADRIAN P.J. MOLLO, ESQ. IN SUPPORT OF OPENING CLAIM CONSTRUCTION BRIEF OF PLAINTIFF LG DISPLAY CO., LTD.

- I, Adrian P. Mollo, Esq. declare under penalty of perjury as follows:
- 1. I am a partner with the McKenna Long & Aldridge LLP. I have personal knowledge of the facts stated in this declaration, and if called as a witness, could competently testify to them. I make this declaration in support of the Opening Claim Construction Brief of LG Display Co., Ltd. ("LGD").
- 2. Attached as Exhibit L-1 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 5,019,002, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 3. Attached as Exhibit L-2(a) is a true and correct copy of the June 13, 2006 Claim Construction Order, issued in the matter of LG. Philips LCD Co., Ltd. v. Chunghwa Picture Tubes Ltd., et al., C.A. No. 05-292-JJF.

- Attached as Exhibit L-2(b) is a true and correct copy of the June 13, 2006 4. Claim Construction Memorandum, issued in the matter of LG. Philips LCD Co., Ltd. v. Chunghwa Picture Tubes Ltd., et al., C.A. No. 05-292-JJF.
- Attached as Exhibit L-2(c) is a true and correct copy of U.S. Patent No. 5. 4,820,222.
- Attached as Exhibit L-2(d) is a true and correct copy of the definition of 6. "resistance," as published in the 1980 edition of the Merriam-Webster Dictionary.
- 7. Attached as Exhibit L-3 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 4,624,737, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-4(a) is a true and correct copy of the April 5, 2003 8. Claim Construction Order, issued in the matter of LG. Philips LCD Co., Ltd. v. Tatung Co. of America, et al., Case No. CV 02-6775 CBM (JTLx) (C.D. Cal.).
- 9. Attached as Exhibit L-4(b) are true and correct excerpts from the December 23, 2003 "Second Revised Joint Claim Construction Statement" filed in the matter of LG. Philips LCD Co., Ltd. v. Tatung Co. of America, et al., Case No. CV 02-6775 CBM (JTLx) (C.D. Cal.).
- 10. Attached as Exhibit L-4(c) is a true and correct copy of the definition of "forming," as published in the 1980 edition of the Merriam-Webster Dictionary.
- 11. Attached as Exhibit L-5 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 5,825,449, together with true and

accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.

- 12. Attached as Exhibit L-6(a) is a true and correct copy of the April 5, 2003

 Claim Construction Order, issued in the matter of *LG.Philips LCD Co., Ltd. v. Tatung Co. of America, et al.*, Case No. CV 02-6775 CBM (JTLx) (C.D. Cal.).
- 13. Attached as Exhibit L-6(b) are true and correct excerpts from the December 23, 2003 "Second Revised Joint Claim Construction Statement" filed in the matter of LG. Philips LCD Co., Ltd. v. Tatung Co. of America, et al., Case No. CV 02-6775 CBM (JTLx) (C.D. Cal.).
- 14. Attached as Exhibit L-6(c) is a true and correct copy of the definition of "one," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 15. Attached as Exhibit L-6(d) is a true and correct copy of the definition of "bonding pad," as published in the 1998 edition of the Penguin Dictionary of Electronics, 3rd Ed.
- 16. Attached as Exhibit L-6(e) is a true and correct copy of the October 23, 2006 Claim Construction Order, issued in the matter of *LG.Philips LCD Co., Ltd. v. Tatung Co. of America, et al.*, Case No. CV 02-6775 CBM (JTLx) (C.D. Cal.).
- 17. Attached as Exhibit L-7 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 5,905,274, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 18. Attached as Exhibit L-8(a) is a true and correct copy of an excerpt of the prosecution history of U.S. Patent No. 6,340,610.

- 19. Attached as Exhibit L-9 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,815,321, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 20. Attached as Exhibit L-10 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 7,176,489, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 21. Attached as Exhibit L-11 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,664,569, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 22. Attached as Exhibit L-12 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 7,218,374, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 23. Attached as Exhibit L-13(a) is a true and correct copy of the definition of "contiguous," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 24. Attached as Exhibit L-13(b) is a true and correct copy of the definition of "continuous," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 25. Attached as Exhibit L-13(c) is a true and correct copy of the definition of "preparing," as published in the 1994 edition of the Merriam-Webster Dictionary.

- Attached as Exhibit L-14 is a is a true and correct copy of LGD's proposed 26. construction of disputed terms from U.S. Patent No. 6,803,984, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-15(a) is a true and correct copy of the definition of 27. "line," as published in the 1994 edition of the Merriam-Webster Dictionary.
- Attached as Exhibit L-15(b) is a true and correct copy of the definition of 28. "portion," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 29. Attached as Exhibit L-15(c) is a true and correct copy of the definition of "step," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 30. Attached as Exhibit L-15(d) is a true and correct copy of the definition of "serial," as published in the 1994 edition of the Merriam-Webster Dictionary.
- Attached as Exhibit L-15(e) is a true and correct copy of the definition of 31. "assembling," as published in the 1994 edition of the Merriam-Webster Dictionary.
- Attached as Exhibit L-16 is a is a true and correct copy of LGD's proposed 32. construction of disputed terms from U.S. Patent No. 7,101,069, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 33. Attached as Exhibit L-17 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,976,781, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.

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- Attached as Exhibit L-18 is a is a true and correct copy of LGD's proposed 34. construction of disputed terms from U.S. Patent No. 7,125,157, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-19(a) is a true and correct copy of the definition of 35. "adjacent," as published in the 1994 edition of the Merriam-Webster Dictionary.
- Attached as Exhibit L-19(b) is a true and correct copy of the definition of 36. "contact," as published in the 1994 edition of the Merriam-Webster Dictionary.
- Attached as Exhibit L-19(c) is a true and correct copy of the definition of 37. "opposite," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 38. Attached as Exhibit L-20 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,689,629, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-21(a) is a true and correct copy of the definition of 39. "dummy," as published in the 2000 edition of "The Authoritative Dictionary of IEEE Standards Terms (Seventh Edition)".
- Attached as Exhibit L-22 is a is a true and correct copy of LGD's proposed 40. construction of disputed terms from U.S. Patent No. 5,748,266, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 41. Attached as Exhibit L-23 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,734,944, together with true and

accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.

- Attached as Exhibit L-24 is a is a true and correct copy of LGD's proposed 42. construction of disputed terms from U.S. Patent No. 6,778,160, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-25 is a is a true and correct copy of LGD's proposed 43. construction of disputed terms from U.S. Patent No. 7,090,506, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 44. Attached as Exhibit L-26 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,734,926, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-27 is a true and correct copy of the definition of "gap," 45. as published in the 1994 edition of the Merriam-Webster Dictionary.
- 46. Attached as Exhibit L-28 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,134,092, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- Attached as Exhibit L-29 is a true and correct copy of the definition of 47. "diffuse," as published in the 1994 edition of the Merriam-Webster Dictionary.

- 48. Attached as Exhibit L-30 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,013,923, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 49. Attached as Exhibit L-31 is a true and correct copy of the definition of "short circuit," as published in the 1994 edition of the Merriam-Webster Dictionary.
- 50. Attached as Exhibit L-32 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 5,619,352, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 51. Attached as Exhibit L-33 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 6,008,786, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.
- 52. Attached as Exhibit L-34 is a is a true and correct copy of LGD's proposed construction of disputed terms from U.S. Patent No. 7,280,179, together with true and accurate excerpts from LGD's evidence (with select emphasis added in the form of highlighting) in support of its proposed constructions.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on this 11th day of August, 2008.

Adrian P.J. Mollo

EXHIBIT L-1

Ex. L-1 LGD US PATENT No. 5,019,002

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	PAGE
substrate	16
forming a pattern of pixels on said substrate	16
forming a plurality of row and column intersecting pixel activation lines	22
interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another	1
interconnecting	1
substantially all	1
row lines	22
column lines	22
row and column lines	22
outer electrostatic discharge guard ring	1
resistance	1
to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays	24
protection from electrostatic discharges	24
row and column activation lines	22
removing said outer guard ring and row and column interconnections	33
removing	33
inner electrostatic discharge guard ring	24
shunt switching elements	16

EXHIBIT L-1 U.S. PATENT NO. 5,019,002 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising: providing a substrate; forming a pattern of pixels on said substrate;



forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another; forming an outer electrostatic discharge guard ring

on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

LGD's Claim Construction

interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another - electrically connecting with conductive material all or nearly all row lines to at least one other row line and electrically connecting with conductive material all or nearly all of the column lines to at least one other column line

interconnecting - electrically connecting with conductive material

substantially all - all or nearly

outer electrostatic discharge **guard ring** – a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharge

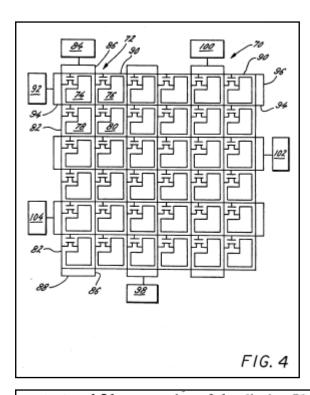
resistance - a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING SUBSTANTIALLY ALL OF SAID ROW LINES TO ONE ANOTHER AND SUBSTANTIALLY ALL OF SAID **COLUMN LINES TO ONE ANOTHER":**

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid

1:34-46

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING SUBSTANTIALLY ALL OF SAID ROW LINES TO ONE ANOTHER AND SUBSTANTIALLY ALL OF SAID COLUMN LINES TO ONE ANOTHER" (cont'd):



contact pad 84 at one edge of the display 70. A second column (source) line or bus 86 connects the subpixels 76 and 80 and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad 84. The bus lines 82 and 86 are interconnected (shorted) at or before the pad 84 and are interconnected (shorted) at the opposite ends by a line or short 88.

the pixels to the row pad 92. The bus lines 90 and 94 are interconnected (shorted) at or before the pad 92 and are interconnected (shorted) at the opposite ends by a line or short 96.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads 98 and 100, etc. The pads 84, 98 and 100 are illus5.61-68

6:6-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING SUBSTANTIALLY ALL OF SAID ROW LINES TO ONE ANOTHER AND SUBSTANTIALLY ALL OF SAID COLUMN LINES TO ONE ANOTHER" (cont'd)

To avoid the fatal defect of the multiple open lines, as also disclosed in U.S. Ser. No. 948,224, the redundant row and column bus lines can be further interconnected at each subpixel. Each pair of the column bus lines 82 and 86 are additionally interconnected between each of the subpixels 74, 78, etc. by respective lines or shorts. In

6:38-43

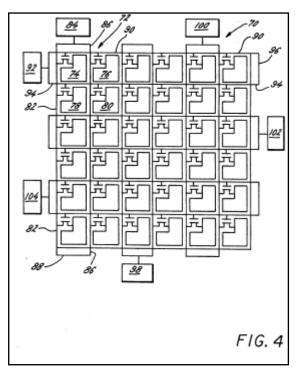
The ESD preventive structure can also include an outer ESD guard ring 200, best illustrated in FIG. 7. Only one corner portion 202 of the display and guard ring 200 is illustrated. While the display is being manufactured, the outer guard ring 200 is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines 204 and 206. A corner pad 208 is con-

8:1-8

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors 146, 194 and 222, etc. also can be formed as other active switching elements, such as diodes. It is

8.49-59

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING":



contact pad 84 at one edge of the display 70. A second column (source) line or bus 86 connects the subpixels 76 and 80 and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad 84. The bus lines 82 and 86 are interconnected (shorted) at or before the pad 84 and are interconnected (shorted) at the opposite ends by a line or short 88.

5:61-68

the pixels to the row pad 92. The bus lines 90 and 94 are interconnected (shorted) at or before the pad 92 and are interconnected (shorted) at the opposite ends by a line or short 96.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads 98 and 100, etc. The pads 84, 98 and 100 are illus-

6:6-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING" (cont'd):

The ESD preventive structure can also include an outer ESD guard ring 200, best illustrated in FIG. 7. Only one corner portion 202 of the display and guard ring 200 is illustrated. While the display is being manufactured, the outer guard ring 200 is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines 204 and 206. A corner pad 208 is con-

8:1-8

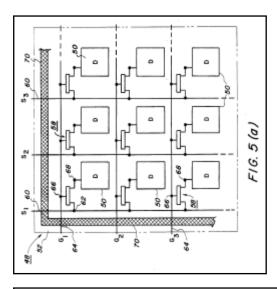
Hynecele or view of Harrison and Mack et al. Tuan discloses an electro-static discharge protection network with interconnecting resistance elements but does not teach means for removing the same at the completion of the device manufacture. Harrison teaches an external buffer net-

Appl. No. 07/218,312, OA mailed 03/31/89, p. 3

Tuan in Fig. 5(a) is concerned with Harrison and Mack. electrostatic discharge protection of an active matrix display. The resistive stripes 70 are not however removable as required by independent claims 1 and 19, as noted by the Examiner.

Appl. No. 07/218,312, 07/12/1990 Proposed Response, p. 2

INTRINSIC EVIDENCE FOR DISPUTED TERM "INTERCONNECTING" (cont'd):



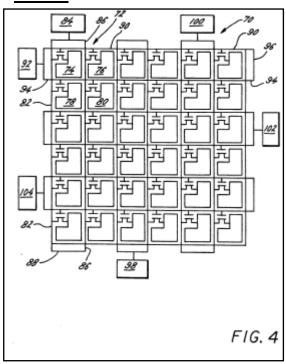
The two major advantages of this configuration are: first, the resistive stripe 46 may be fabricated simultaneously with the deposition of the n+ a-Si:H source and drain layers; and, second, that the resistive stripe is located on the substrate at a location where it will not compete for real estate. It should be understood that the resistive stripe may be fabricated of lightly doped or undoped a-Si:H if desired, in order to be consistent with, and to be deposited simultaneously with, other device layers. N+ a-Si:H is particularly appealing because its resistivity is approximately 102 ohm-cm and in thin film form it is not uncommon to make resistors in the range of 107 to 109 ohms.

USP 4,803,536, 4:45-57

then to the display electrode 50. All the source lines (S1 to S_N) and all the gates lines $(G_1 \text{ to } G_N)$ are shown connected together with suitable resistors, for example, n+ a-Si:H resistive stripes 70. By following the principles of resistive value selection set forth above, a protective network will be effected which will protect the gate dielectrics of all the switching transistors from electrostatic discharge but will have no effect on normal operation.

USP 4,803,536, 5:30-39

INTRINSIC EVIDENCE FOR DISPUTED TERM "SUBSTANTIALLY



contact pad 84 at one edge of the display 70. A second column (source) line or bus 86 connects the subpixels 76 and 80 and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad 84. The bus lines 82 and 86 are interconnected (shorted) at or before the pad 84 and are interconnected (shorted) at the opposite ends by a line or short 88.

5:61-68

the pixels to the row pad 92. The bus lines 90 and 94 are interconnected (shorted) at or before the pad 92 and are interconnected (shorted) at the opposite ends by a line or short 96.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads 98 and 100, etc. The pads 84, 98 and 100 are illus-

6:6-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "SUBSTANTIALLY ALL" (cont'd):

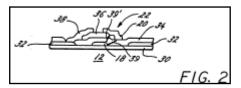
Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid

1:34-46

The ESD preventive structure can also include an outer ESD guard ring 200, best illustrated in FIG. 7. Only one corner portion 202 of the display and guard ring 200 is illustrated. While the display is being manufactured, the outer guard ring 200 is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines 204 and 206. A corner pad 208 is con-

8:1-8

INTRINSIC EVIDENCE FOR DISPUTED TERM "OUTER ELECTROSTATIC DISCHARGE GUARD RING":



During manufacture of the device 10, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20. The discharge frequently will result in a short 39 through the insulator 34 or a short 39' through the insulator 34 and the silicon layer 36 in the transistor 22, between the adjacent crossover points of the lines 18 and 20 as can be seen in FIG. 2. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device 10, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device 10 does not provide any redundancy or subpixels and hence the defect cannot easily be isolated.

4.46-58

Page 13 of 39

INTRINSIC EVIDENCE FOR DISPUTED TERM "OUTER ELECTROSTATIC DISCHARGE GUARD RING" (cont'd):

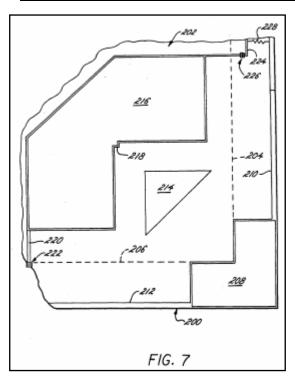


FIG. 7 is a partial plan view of one embodiment of an exterior ESD guard ring of the present invention.

The ESD preventive structure can also include an outer ESD guard ring 200, best illustrated in FIG. 7. Only one corner portion 202 of the display and guard ring 200 is illustrated. While the display is being manufactured, the outer guard ring 200 is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines 204 and 206. A corner pad 208 is con-

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter. 3:20-21

8:1-8

1:8-14

2:45-51

INTRINSIC EVIDENCE FOR DISPUTED TERM "OUTER **ELECTROSTATIC DISCHARGE GUARD RING" (cont'd):**

ter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

2.61-68

Each pixel 112, 114, 116 and 118 includes a respective active element, such as transistors 136, 138, 140 and 142 which couple the pixels to the respective source lines 120 or 124 and gate lines 128 or 130. To prevent a large electrostatic potential discharging through one of the transistors 136, 138, 140 and 142, an internal ESD guard ring 144 is formed around the pixels 112, 114, 116 and 118. The guard ring 144 is illustrated as a closed ring, but could also be an open L or C-shaped line if the gate and source pads all are on one respective side of the display 110.

7:11-21

228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228 provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line 210 and the other set of gate or source lines. The

8:26-34

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt

8.49-57

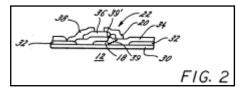
INTRINSIC EVIDENCE FOR DISPUTED TERM "RESISTANCE":

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

1:8-14

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at

2.52-64



During manufacture of the device 10, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20. The discharge frequently will result in a short 39 through the insulator 34 or a short 39' through the insulator 34 and the silicon layer 36 in the transistor 22, between the adjacent crossover points of the lines 18 and 20 as can be seen in FIG. 2. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device 10, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device 10 does not provide any redun-

4:46-58

INTRINSIC EVIDENCE FOR DISPUTED TERM "RESISTANCE" (cont'd):

The gate to source or drain shorts referred to above in discussing the dielectric 58, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric 58, but will not be eliminated. The potential can be high enough to again form a short 69 through the gate insulator 52 and the semiconductor material 54 in the transistor 40, between the source 60 and the gate 50. Depending upon the display structure, at least one pixel or one subpixel (FIG. 4) will be defective.

5:33-43

120 or 124 and gate lines 128 or 130. To prevent a large electrostatic potential discharging through one of the transistors 136, 138, 140 and 142, an internal ESD guard ring 144 is formed around the pixels 112, 114, 116 and 118. The guard ring 144 is illustrated as a closed ring,

7:14-18

In operation, with the guard ring 144, a potential placed upon the source pads 122 will not short one of the transistors 136 or 140. Instead, the transistor 146 will turn on followed by the transistor 150, shorting the potential from the pad 122, via the line 120, the transistor 146, the guard ring 144, the transistor 150 and the line 128 to the pad 132. Thus, the guard ring 144 will not allow high potentials across the pads 122, 126, 132 and 134. The guard ring 144 preferably is formed concurrently with the display elements and is not removed, providing continuous protection even following manufacture of the display 110.

7:35-46

An internal ESD guard ring 192 is coupled via a transistor structure 194 to the source line 174 and via a transistor structure 196 to the gate line 190. The guard ring 192 and transistors 194 and 196 operate as before described to short any potential to ground. The low value of the normal operating voltages does not turn on the transistors 194 and 196, which do not effect the normal display operation.

7:61-68

INTRINSIC EVIDENCE FOR DISPUTED TERM "RESISTANCE" (cont'd):

and removed along the line 206. The line 210 is connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228 provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line 210 and the other set of gate or source lines. The resistance 228 minimizes the discharge current surge and the shunt transistors 222 and 226 act as before described. There will be at least one corner backplane pickup pad 216 and preferably there will be two or three, each with their associated shunt transistors.

8:23-37

EXTRINSIC EVIDENCE FOR DISPUTED TERM "RESISTANCE":

re-eis-tance \ri-'zis-ton(t)s\ n 1 a: an act or instance of resisting corrownton b: a means of resisting 2: the ability to resist; exp: the inherent capacity of a living being to resist untoward circumstances (as disease, malnutrition, or toxic agents) 3: an opposing or retarding force 4 a: the opposition offered by a body or substance to the passage through it of a steady electric current b: a source of resistance b often cap: an underground organization of a conquered country engaging in sabotage and secret operations against occupation forces and collaborators

"Resistance." Def. 4a. Merriam-Webster's Collegiate Dictionary. 10th ed. 1980

EXHIBIT U.S. PATENT NO. 5.019.002 TERMS IN DISPUTE

ASSERTED CLAIM 1

 A method of manufacturing active matrix display backplanes and displays therefrom, comprising: providing a substrate; forming a pattern of pixels on said substrate;



forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display,

ASSERTED CLAIM 8

8. The method as defined in claim 1 including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

LGD's Claim Construction

substrate - the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support

forming a pattern of pixels on said substrate - depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate

shunt switching elements shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes

¹ Disputed Term "substrate" also appears in asserted claim 8 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERM "SUBSTRATE":

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and

1:34-38

357, 1981. The device 10 includes a substrate 12, sets of contact pads 14 and 16, sets of control or bus lines 18 and 20, and, in this particular example of the prior art, transistors 22 and pixel back contacts 24.

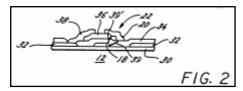
The substrate 12 commonly employed in these devices is formed from glass. The control lines 18 and 20

3:33-38

Referring in detail to FIG. 2, several problems occur when the switching element, transistor 22 is manufactured. The substrate 12 is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid

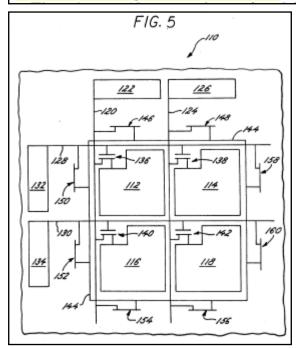
4:9-13

INTRINSIC EVIDENCE FOR DISPUTED TERM "FORMING A PATTERN OF PIXELS ON SAID SUBSTRATE":



357, 1981. The device 10 includes a substrate 12, sets of contact pads 14 and 16, sets of control or bus lines 18 and 20, and, in this particular example of the prior art, transistors 22 and pixel back contacts 24.





Referring now to FIG. 5, a matrix display incorporating one embodiment of an internal ESD guard ring of the present invention is designated generally by the reference numeral 110. The matrix display 110 is illustrated having four pixels 112, 114, 116 and 118. The pixels, however, can be subdivided into numerous subpixel configurations such as two or four subpixels, two by four or six subpixels or in three subpixels for color display applications. Also, as previously stated for the

subpixel matrix display 70, the number of pixels can be of any number and configuration, square or rectangular.

6:60-7:2

INTRINSIC EVIDENCE FOR DISPUTED TERM "FORMING A PATTERN OF PIXELS ON SAID SUBSTRATE" (cont'd):

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid

1:34-46

of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

1:52-55

At each matrix crossover point 26, where a row line 18 and a column line 20 cross, a switching element, transistor 22 is formed to connect the row line 18 and column line 20 to the pixel back contacts 24. The active medium is deposited at least on the contacts 24 which will optically change properties in response to the combined voltages or currents in the respective crossover point 26 formed by the row 18 and column 20. The active medium at a given crossover point 26 will appear as a square or dot in the overall checkerboard type matrix of the display 10. The actual size of the transis-

3:47-57

suppression layer 30. An ITO layer 32 is formed and etched to provide an ITO free area on which the gate 18 is deposited. Following the deposition of the gate 18, a gate insulator layer 34 is deposited. Although a smooth

4:20-23

An amorphous silicon layer 36 is then deposited, with the source 20 and a drain 38 deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor 22. During operation the activation of the source 20 and the gate 18 couples power through the silicon alloy 36 to the drain and hence to the contact pad 24 formed by the ITO layer 32.

4:38-45

INTRINSIC EVIDENCE FOR DISPUTED TERM "FORMING A PATTERN OF PIXELS ON SAID SUBSTRATE" (cont'd):

During all of the transistor processing steps, the refractory metal layer 48 remains over a pixel contact pad 68 upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad 68 leaving the ITO layer 46 exposed after all the processing has been completed.

5.24 - 32

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors 146, 194 and 222, etc. also can be formed as other active switching elements, such as diodes. It is

8:49-59

INTRINSIC EVIDENCE FOR DISPUTED TERM "SHUNT SWITCHING ELEMENTS":

The ESD guard ring 144 preferably is formed from a low resistance metal, such as an aluminum alloy. The transistors 146 through 160 can include a floating gate (not illustrated), no gate, or can include an oxide below to form a spark gap.

7:29-34

GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors 146, 194 and 222, etc. also can be formed as other active switching elements, such as diodes. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

8:55-62

EXHIBIT U.S. PATENT NO. 5,019,002 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising: providing a substrate; forming a pattern of pixels on said substrate;



forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

ASSERTED CLAIM 8

8. The method as defined in claim 1 including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

LGD's Claim Construction

forming a plurality of row and column intersecting pixel activation lines - depositing and etching electrically conductive material patterned in rows and columns that control pixels

row lines – electrically conductive material patterned in rows that control pixels

column lines - electrically conductive material patterned in columns that control pixels

row and column lines electrically conductive material patterned in rows and columns that control pixels

row and column activation lines - electrically conductive material patterned in rows and columns that control pixels

EVIDENCE FOR DISPUTED TERMS PERTAINING TO "ROW" AND "COLUMN LINES":

strate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a

1:38-42

vices is formed from glass. The control lines 18 and 20 are organized into a matrix of rows 18 and columns 20. The control line rows 18 in this device 10 serve as gate electrodes and the control line columns 20 as source connections. One contact pad 14 is connected to one end of each of the row control lines 18. One contact pad 16 is connected to one end of each of the column control lines 20. The display drive control (not shown) is

3:38-45

EXHIBIT ___ U.S. PATENT NO. 5,019,002 TERMS IN DISPUTE

ASSERTED CLAIM 8

8. The method as defined in claim 1 including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

LGD's Claim Construction

to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays - to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display

protection from electrostatic discharges - to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display

inner electrostatic discharge guard ring - a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to provide protection from electrostatic discharge

INTRINSIC EVIDENCE FOR DISPUTED TERM "TO PROVIDE PROTECTION FROM ELECTROSTATIC DISCHARGES BETWEEN SAID ROW AND COLUMN ACTIVATION LINES DURING MANUFACTURE OF THE DISPLAYS":

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

1.8-14

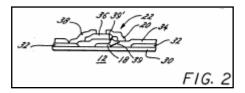
There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter.

2:45-51

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at

2:52-64

INTRINSIC EVIDENCE FOR DISPUTED TERM "TO PROVIDE PROTECTION FROM ELECTROSTATIC DISCHARGES BETWEEN SAID ROW AND COLUMN ACTIVATION LINES DURING MANUFACTURE OF THE DISPLAYS" (cont'd):



During manufacture of the device 10, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20. The discharge frequently will result in a short 39 through the insulator 34 or a short 39' through the insulator 34 and the silicon layer 36 in the transistor 22, between the adjacent crossover points of the lines 18 and 20 as can be seen in FIG. 2. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device 10, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device 10 does not provide any redun-

4:46-58

The gate to source or drain shorts referred to above in discussing the dielectric 58, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric 58, but will not be eliminated. The potential can be high enough to again form a short 69 through the gate insulator 52 and the semiconductor material 54 in the transistor 40, between the source 60 and the gate 50. Depending upon the display structure, at least one pixel or one subpixel (FIG. 4) will be defective.

5.33-43

120 or 124 and gate lines 128 or 130. To prevent a large electrostatic potential discharging through one of the transistors 136, 138, 140 and 142, an internal ESD guard ring 144 is formed around the pixels 112, 114, 116 and 118. The guard ring 144 is illustrated as a closed ring,

7:14-18

INTRINSIC EVIDENCE FOR DISPUTED TERM "TO PROVIDE PROTECTION FROM ELECTROSTATIC DISCHARGES BETWEEN SAID ROW AND COLUMN ACTIVATION LINES DURING MANUFACTURE OF THE DISPLAYS" (cont'd):

and removed along the line 206. The line 210 is connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228 provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line 210 and the other set of gate or source lines. The resistance 228 minimizes the discharge current surge and the shunt transistors 222 and 226 act as before described. There will be at least one corner backplane

8:23-37

INTRINSIC EVIDENCE FOR DISPUTED TERM "PROTECTION FROM ELECTROSTATIC DISCHARGES":

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

1:8-14

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter.

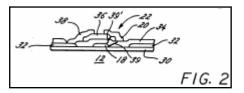
2:45-51

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at

2:52-64

Page 31 of 39

INTRINSIC EVIDENCE FOR DISPUTED TERM "PROTECTION FROM ELECTROSTATIC DISCHARGES" (cont'd):



During manufacture of the device 10, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines 18 and the source lines 20. The discharge frequently will result in a short 39 through the insulator 34 or a short 39' through the insulator 34 and the silicon layer 36 in the transistor 22, between the adjacent crossover points of the lines 18 and 20 as can be seen in FIG. 2. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device 10, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device 10 does not provide any redun-

4:46-58

The gate to source or drain shorts referred to above in discussing the dielectric 58, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric 58, but will not be eliminated. The potential can be high enough to again form a short 69 through the gate insulator 52 and the semiconductor material 54 in the transistor 40, between the source 60 and the gate 50. Depending upon the display structure, at least one pixel or one subpixel (FIG. 4) will be defective.

5:33-43

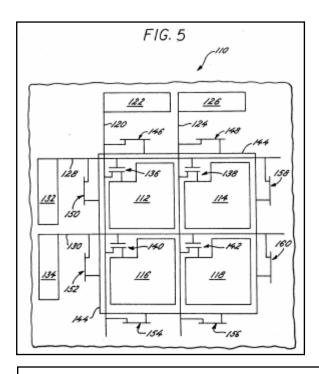
120 or 124 and gate lines 128 or 130. To prevent a large electrostatic potential discharging through one of the transistors 136, 138, 140 and 142, an internal ESD guard ring 144 is formed around the pixels 112, 114, 116 and 118. The guard ring 144 is illustrated as a closed ring,

7:14-18

INTRINSIC EVIDENCE FOR DISPUTED TERM "PROTECTION FROM ELECTROSTATIC DISCHARGES" (cont'd):

and removed along the line 206. The line 210 is connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228 provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line 210 and the other set of gate or source lines. The resistance 228 minimizes the discharge current surge and the shunt transistors 222 and 226 act as before described. There will be at least one corner backplane 8:23-37

INTRINSIC EVIDENCE FOR DISPUTED TERM "INNER ELECTROSTATIC DISCHARGE GUARD RING":



Referring now to FIG. 5, a matrix display incorporating one embodiment of an internal ESD guard ring of the present invention is designated generally by the reference numeral 110. The matrix display 110 is illustrated having four pixels 112, 114, 116 and 118. The pixels, however, can be subdivided into numerous subpixel configurations such as two or four subpixels, two by four or six subpixels or in three subpixels for color display applications. Also, as previously stated for the

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subpixel matrix display 70, the number of pixels can be of any number and configuration, square or rectangular.

6:60-7:2

INTRINSIC EVIDENCE FOR DISPUTED TERM "INNER ELECTROSTATIC DISCHARGE GUARD RING" (cont'd)

The gate to source or drain shorts referred to above in discussing the dielectric 58, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric 58, but will not be eliminated. The potential can be high enough to again form a short 69 through the gate insulator 52 and the semiconductor material 54 in the transistor 40, between the source 60 and the gate 50. Depending upon the display structure, at least one pixel or one subpixel (FIG. 4) will be defective.

5:33-43

Each pixel 112, 114, 116 and 118 includes a respective active element, such as transistors 136, 138, 140 and 142 which couple the pixels to the respective source lines 120 or 124 and gate lines 128 or 130. To prevent a large electrostatic potential discharging through one of the transistors 136, 138, 140 and 142, an internal ESD guard ring 144 is formed around the pixels 112, 114, 116 and 118. The guard ring 144 is illustrated as a closed ring, but could also be an open L or C-shaped-line if the gate and source pads all are on one respective side of the display 110.

7:11-22

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt

8:49-57

EXHIBIT ____ U.S. PATENT NO. 5,019,002 TERMS IN DISPUTE

ASSERTED CLAIM 1

 A method of manufacturing active matrix display backplanes and displays therefrom, comprising: providing a substrate; forming a pattern of pixels on said substrate;

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forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

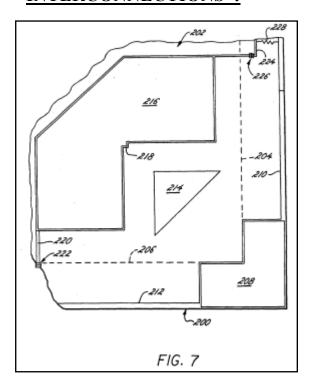
removing said outer guard ring and row and column interconnections prior to completion of the display,

LGD's Claim Construction

removing said outer guard ring and row and column interconnections- physically disconnecting said guard ring and row and column interconnections

removing – physically disconnecting said guard ring and row and column interconnections

INTRINSIC EVIDENCE FOR DISPUTED TERM "REMOVING SAID OUTER GUARD RING AND ROW AND COLUMN INTERCONNECTIONS":



guard ring 200. The L-shaped corner pad 208 can be grounded and also provides the alignment for the scribe lines 204 and 206, which are utilized to disconnect the source and gate jumpers and the guard ring 200 after the structure is completed. The corner portion 202 includes

8:11-16

The outer guard ring lines 210 and 212 preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring 44 and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines 204 and 206 can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

8:40-48

INTRINSIC EVIDENCE FOR DISPUTED TERM "REMOVING SAID **OUTER GUARD RING AND ROW AND COLUMN INTERCONNECTIONS"** (cont'd):

ter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

2:62-68

228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228

8:27-30

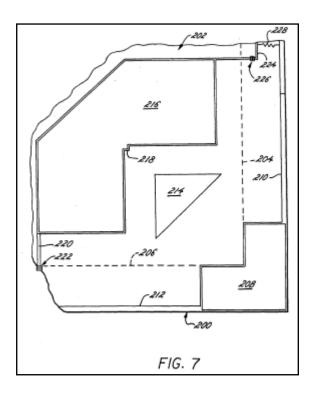
The outer guard ring lines 210 and 212 preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring 44 and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines 204 and 206 can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

8:40-48

supply such a teaching. Hynecek removes the interconnect 4 between devices 3, but does not provide row and column line connections or remove such connection if resistance 11 is taken to be such a connection. Likewise, Harrison is an integrated circuit, which has elements which could be separated at score line 270, but the elements are not an outer discharge ring connected as claimed. Tuan as noted in column 1 thereof, was

Appl. No. 07/218,312, 07/12/1990 Proposed Response, p. 2

INTRINSIC EVIDENCE FOR DISPUTED TERM "REMOVING":



guard ring 200. The L-shaped corner pad 208 can be grounded and also provides the alignment for the scribe lines 204 and 206, which are utilized to disconnect the source and gate jumpers and the guard ring 200 after the structure is completed. The corner portion 202 includes

8:11-16

The outer guard ring lines 210 and 212 preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring 44 and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines 204 and 206 can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

8:40-48

INTRINSIC EVIDENCE FOR DISPUTED TERM "REMOVING" (cont'd):

ter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

2:62-68

228, such as 100 K ohms (illustrated schematically). The outer ESD guard ring 200 provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance 228

8:27-30

The outer guard ring lines 210 and 212 preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring 44 and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines 204 and 206 can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

8:40-48

EXHIBIT L-2(a)

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

LG. PHILIPS LCD CO. LTD,

v.

:

Plaintiff,

:

Civil Action No. 05-292-JJF

TATUNG COMPANY, TATUNG COMPANY
OF AMERICA, INC., CHUNGWHA
PICTURE TUBES LTD., and
VIEWSONIC CORP.,

:

Defendants.

ORDER

At Wilmington, this B Day of June, 2006, for the reasons set forth in the Memorandum Opinion issued this date,

IT IS HEREBY ORDERED that for the purposes of United States

Patent No. 6,738,121, the following terms and phrases are

construed as follows:

- 1. The term "interconnecting," as used in claim 1, means "electrically connecting with conductors;"
- 2. The phrase "removing said outer guard ring and row and column interconnections," as used in claims 1 and 12, means "physically disconnecting said guard ring and row and column interconnections;"
- 3. The term "outer electrostatic discharge guard ring," as used in claims 12, 19, and 30, means "a closed or open ring, or

open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges;"

- 4. The term "resistance," as used in claims 1, 2, 3, 12, 13, 14, 19, 20, 21, 30, 31, and 32, means "a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from electrostatic discharge;"
- 5. The term "corner pad," as used in claims 7, 18, 25, and 36, means "an area of conductive material;"
 - 6. The Court declines to construe the term "pickup pad."

UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

LG. PHILIPS LCD CO. LTD,

laintiff

.

Plaintiff,

v. : Civil Action No. 05-292-JJF

:

TATUNG COMPANY, TATUNG COMPANY
OF AMERICA, INC., CHUNGWHA
PICTURE TUBES LTD., and
VIEWSONIC CORP.,

:

Defendants.

Richard D. Kirk, Esquire of THE BAYARD FIRM, Wilmington, Delaware.

Of Counsel: Gaspare J. Bono, Esquire, Matthew T. Bailey, Esquire, and Cass W. Christenson, Esquire of MCKENNA LONG & ALDRIDGE LLP, Washington, D.C..

Attorneys for Plaintiff.

Robert W. Whetzel, Esquire and Matthew W. King, Esquire of RICHARDS, LAYTON & FINGER, Wilmington, Delaware.

Of Counsel: Christine A. Dudzik, Esquire and Thomas W. Jenkins, Esquire of HOWREY LLP, Chicago, Illinois; Julie S. Gabler,

Esquire of HOWREY LLP, Chicago, Illinois; Julie S. Gabler, Esquire of HOWREY LLP, Los Angeles, California; and Glen W. Rhodes, Esquire, J. James Li, Esquire, and Qin Shi, Esquire of HOWREY LLP, San Francisco, California.

Attorneys for Defendants.

MEMORANDUM OPINION

June 13, 2006
Wilmington, Delaware

Farnan, District Judge:

Plaintiff L.G. Philips LCD Co., LTD ("LPL") filed this patent infringement action against Defendants Tatung Company,
Tatung Company of America, Inc., Chungwha Picture Tubes, LTD.,
and ViewSonic Corporation (collectively "CPT"). LPL alleges that
CPT has infringed U.S. Patent No. 5,019,002 ("the '002 patent").
LPL's Complaint (D.I. 1) also alleges infringement of U.S.
Patent No. 6,738,121 ("the '121 patent"), but LPL has withdrawn
all claims relating to that patent. (D.I. 180.) Presently
before the Court is the claim construction dispute of the
parties. The parties briefed their respective positions, and the
Court held a Markman hearing on March 20, 2006. This Memorandum
Opinion provides the Court's construction of the claim terms and
phrases disputed by the parties.

BACKGROUND

The Patent at issue in this lawsuit relates to flat panel, display screens and methods of manufacturing them that include electrostatic discharge guard rings to protect the active elements of the display from electrostatic discharge during and after manufacturing. In their briefing and at the Markman hearing, the parties disputed twenty-six terms and phrases from the claims of both the '002 patent and the '121 patent. By its Order dated March 22, 2006 (D.I. 155), the Court ordered the parties to select a reduced number of terms and phrases to be

construed by the Court. The Court allowed LPL to submit a maximum of five terms or phrases and CPT a maximum of eight.

(D.I. 155.) Following the parties' submissions of the terms and phrases to be construed, LPL filed a Notice Of Voluntary

Withdrawal Of Claims Relating To U.S. Patent No. 6,738,121 (D.I. 180). As a result of that withdrawal and the fact that one claim term was submitted by both parties, there are currently six claim terms and phrases in dispute: "interconnecting," "outer electrostatic discharge guard ring," "resistance," "corner pad," "removing said outer guard ring and row and column interconnections," and "pickup pad."

DISCUSSION

I. Legal Principles Of Claim Construction

Claim construction is a question of law. Markman v.

Westview Instruments, Inc., 52 F.3d 967, 977-78 (Fed. Cir. 1995),

aff'd, 517 U.S. 370, 388-90 (1996). In interpreting a claim, a

court should look first to the intrinsic evidence, i.e. the

patent itself, including the claims and the rest of the

specification, and, if in evidence, the prosecution history.

Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.

Cir. 1996). Although it is within the sound discretion of a

court to use extrinsic evidence as an aid in construing a claim,

extrinsic evidence is "unlikely to result in a reliable

interpretation of patent claim scope unless considered in the

context of the intrinsic evidence." Phillips v. AWH Corp., 415
F.3d 1303, 1319 (Fed. Cir. 2005) (en banc).

A claim term should be construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Markman, 52 F.3d at 986. However, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1313. Thus, the specification is usually "dispositive; it is the single best guide to the meaning of a disputed term." Id. at 1315 (quoting Vitronics, 90 F.3d at 1582). In other words, a claim term can be given its correct construction only within the context of "what the inventors actually invented and intended to envelop with the claim." Phillips, 415 F.3d at 1316.

II. Construction Of The Disputed Terms and Phrases

The language of independent claim 1 and dependent claims 3 and 7 is representative of the disputed terms and phrases. In full, claim 1 provides (emphasis added):

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:
 providing a substrate;
 forming a pattern of pixels on said substrate;
 forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;
 forming an outer electrostatic discharge quard

ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

('002 patent, col. 8, 1. 65 - col. 9, 1. 12.) In full, claim 3 provides (emphasis added): "3. The method as defined in claim 1 including forming at least one pickup pad coupled to said resistance via a shunt switching element." (Id. col. 9, 11. 16-18.) In full, claim 7 provides (emphasis added): "7. The method as defined in claim 1 including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections." (Id. col. 9, 11. 29-33.)

A. Construction of "Interconnecting"

LPL contends that the term "interconnecting" should be construed as "shorting." (D.I. 135 at 12.) LPL argues that "'interconnecting' was used throughout the entire intrinsic record in a manner consistent with this single meaning." (Id.) CPT contends that "shorting" is impermissibly vague because the specification uses that term in a variety of contexts. (D.I. 144 at 6.) CPT proposes instead the construction "electrically connecting with conductors." (D.I. 164 at 1.)

The Court agrees with CPT that LPL's proposed construction

is vague. Substituting "shorting" for "interconnecting" would not clarify the meaning of "interconnecting," but rather would make it more ambiguous. In the '002 patent's specification, "short" is used in at least four different ways: the path taken by an unintended, destructive discharge of a static potential ('002 patent, col. 2, 11. 57-62); a physical defect in electrical components resulting in an unintended current pathway (Id., col. 4, 11. 27-28); a deliberate re-routing of an electrostatic discharge via a shunt transistor (Id., col. 7, 11. 35-41); and a deliberate connection between electrical elements to provide an alternate current pathway (Id., col. 5, 11. 65-68). Only the last of these is consistent with LPL's proposed construction of "interconnecting".

LPL contends that CPT's proposed construction of "electrically connecting with conductors" improperly limits the term "interconnecting" to a single embodiment by specifying that the electrical connection must be made with conductors. (D.I. 158 at 2.) However, the consistent use of a claim term by the inventor in the specification may serve to limit the scope of a claim. Nystrom v. Trex Co., Inc., 424 F.3d 1136, 1145 (Fed. Cir. 2005). Here, CPT's proposed construction is consistent with the inventor's use of "interconnecting" throughout the '002 patent's

specification.¹ "Interconnecting" is consistently described or illustrated in figures as using "lines", "shorts", or "jumpers", i.e. conductors, to connect electrical elements. (See e.g., '002 patent, col. 5, ll. 65-68; col. 6, ll. 6-9; col. 6, ll. 42-43; col. 8, ll. 5-7.) Therefore, the Court will construe "interconnecting" to mean "electrically connecting with conductors."

B. <u>Construction of "Removing Said Outer Guard Ring and Row and Column interconnections"</u>

LPL contends that the phrase "removing said outer guard ring and row and column interconnections" does not require construction, but that the proper construction, if one is necessary, is "physically disconnecting said guard ring and row and column interconnections." (D.I. 135 at 23-24.) CPT's proposed construction is "electrically disconnecting the interconnections between rows and between columns, and electrically disconnecting rows and columns from the outer guard ring." (D.I. 137 at 12.) The Court agrees with LPL's construction.

The parties' dispute hinges on the meaning of "removing," with LPL contending that it means "physically disconnecting" and

Defendants' proposed construction is also consistent with the use of "interconnecting" in U.S. Patent 4,820,222 ("the '222 patent), which has the same inventor as the '002 patent and is incorporated by reference in the '002 patent. ('002 patent, col. 2, 11. 30-36.)

Defendants contending that it means "electrically disconnecting." CPT's construction depends on its assertion that "removing" means "removing a part or component from an electronic circuit." (D.I. 144 at 3; D.I. 138 at 9.) However, as it is used throughout the specification, "removing" is more logically interpreted as referring to the removal of the guard ring and row and column interconnections from the display panel. (See '002 patent, Abstract ("the external quard ring is removed prior to completion of the display"); col. 2, 11. 64-65 ("the external guard ring is removed at the end of the display manufacturing process"); col. 8, 11. 27-30 ("[t]he outer ESD guard ring . . . is removed prior to completion of the display").) Thus, the intrinsic evidence indicates that "removing" is used to mean physical disconnection and separation such that the outer guard ring and row and column interconnections are not included in the finished display panel. Therefore, the Court will construe "removing said outer guard ring and row and column interconnections" as "physically disconnecting said guard ring and row and column interconnections."

C. <u>Construction of "Outer Electrostatic Discharge Guard Ring"</u>

LPL's proposed construction of the phrase "outer electrostatic discharge guard ring" is "a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges." (D.I. 158 at

2.) CPT's proposed construction is "a ring of conductor, located external to the inner electrostatic discharge guard ring if the two rings are used together, for draining off electrostatic buildup to prevent electrostatic discharge." CPT does not dispute that the outer guard ring is "a closed or open ring, or open L or C-shaped line." (D.I. 144 at 6.) The parties do dispute whether the guard ring functions to prevent electrostatic discharge ("ESD") or only to protect against damage caused by ESD.² The parties also dispute the meaning of "outer."

The specification consistently refers to the function of the ESD guard rings as protecting the active elements of the display from ESD rather than preventing ESD altogether. (See '002 patent, Abstract ("At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines."); col. 2, ll. 61-61 ("An external guard ring can be formed, which provides protection during manufacture of the displays . . ."); col. 8, ll. 27-29 ("The outer ESD guard ring provides ESD protection only during manufacture of the display . . .").) CPT points out that the specification uses the word "prevent" or "preventive" to describe the function of the ESD rings. (D.I. 164 at 4.) However, in

² CPT refers to this dispute as "insignificant," but, nevertheless, maintains the position that the proper construction refers to prevention of ESD rather than protection from ESD. (D.I. 164 at 4.)

both of the locations cited, the specification is referring to the prevention of damage caused by ESD rather than to the prevention of ESD itself.

The central dispute over the phrase "outer electrostatic discharge guard ring" is whether "outer" is used in reference to an inner ESD ring or to the entire display panel. CPT contends that "outer" must refer to the outer guard ring's position relative to the inner guard ring. (D.I. 137 at 8.) This contention is untenable. Independent claims 1 and 19 include an outer ESD guard ring, but no inner ESD guard ring. In the context of those claims, CPT's proposed construction would render the adjective "outer" meaningless.

On the other hand, LPL contends that "outer" refers to the outer guard ring's position relative to the active matrix display. CPT concedes that "active matrix display" as used in the '002 patent and in LPL's proposed construction means the entire finished display panel. (D.I. 164 at 3.) CPT argues that the Court should reject LPL's proposed construction because it is based on "the erroneous notion that the outer ring must be physically removed at the end of the manufacture." (Id.) As the Court concluded in section II.B. above, however, the intrinsic evidence indicates that physical removal of the outer guard ring is precisely what the patent teaches. Therefore, the Court will construe "outer electrostatic discharge guard ring" as "a closed"

or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."

D. Construction of "Resistance"

The parties agree that one of ordinary skill in the art would understand "resistance" to mean a physical property of a material or device characterized by opposition to the flow of electric current. (D.I. 135 at 13; D.I. 137 at 9.) They also agree that in the '002 patent, "resistance" is used to denote a circuit component. (D.I 135 at 13; D.I. 160 at 2.) LPL contends that because "[a]ll circuit components . . . have the characteristic of resistance," the Court should construe "resistance" as "any component used to cause a voltage drop during current flow." (D.I. 135 at 13.) CPT's proposed construction is "[a] resistance, as it is used in the claims, means a resistor, which is a circuit element that has a specified resistance to the flow of electrical current. A resistance does not include switching elements such as transistors and diodes." (D.I. 137 at 9.)

LPL's proposed construction cannot be correct because, as CPT points out, (D.I. 137 at 12), it would exclude the single preferred embodiment that incorporates a "resistance." (See '002 patent, col. 8, ll. 1-48.) The only purposes stated for the "resistance" in that embodiment are to provide an "ESD short for

high electrostatic potentials . . . ," (<u>Id.</u>, col. 8, 1. 31), and to minimize "the discharge current surge . . .," (<u>Id.</u>, col. 8, 1. 35). Thus, "resistance" as used in that embodiment, would not fall within the scope of LPL's proposed construction of "any component used to cause a voltage drop during current flow." A claim construction that excludes a preferred embodiment "is rarely, if ever, correct and would require highly persuasive evidentiary support. . . ." <u>Vitronics Corp. v. Conceptronic, Inc.</u>, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (citations omitted). The Court finds no such evidentiary support in this case.

On the other hand, CPT's proposed construction unnecessarily limits "resistance" to one specific electric component, a resistor. There is no support in the intrinsic record for such a narrow interpretation. Moreover, a person skilled in the art would certainly understand the meaning of "resistor" so it is logical to conclude that the inventor would have chosen that term had he intended to refer only to that specific component.

LPL correctly notes, (D.I. 163 at 3), that it is improper to import limitations from a preferred embodiment into the claims. See JVW Enterprises, Inc. v. Interact Accessories, Inc., 424 F.3d 1324, 1335 (Fed. Cir. 2005). However, "there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." Phillips v. AWH Corp., 415 F.3d 1303, 1323 (Fed.

Cir. 2005) (quoting <u>Comark Communications</u>, <u>Inc. v. Harris Corp.</u>, 156 F.3d 1182, 1186-87 (Fed. Cir. 1998)). Here, because "resistance" is used in the claims in a manner somewhat different from its ordinary meaning to one of skill in the art, the only guidance as to how the Court should construe the term is how it is used in the single embodiment in which it appears. That embodiment mentions a "resistance" three times:

The [ESD guard ring] line 210 is connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228, such as 100 K ohms (illustrated schematically). . . . The resistance provides an ESD short for high electrostatic potentials which can be incurred during manufacturing . . . The resistance minimizes the discharge current surge

('002 patent, col. 8, 11. 23-34.) In the claims, the term "resistance" is used consistently to denote only a circuit component used to couple the outer ESD guard ring to the interconnected row and column lines and the pickup pad. (See e.g. Id., col. 9, 11. 63-65; col. 10, 11. 6-8.)

Reading the claims in light of the specification, which describes the "resistance" only in general terms, the Court concludes that the patentee intended the claims and this embodiment in the specification to be coextensive at least in regard to the term "resistance". Therefore, the Court will

The Court also notes that the patentee explicitly stated that certain elements of the invention could vary from the specific descriptions in that embodiment, but did not include the "resistance" among those elements. ('002 patent, col. 8, 11. 49-

construe "resistance" as "a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge."

E. Construction of "Corner Pad"

LPL contends that the term "corner pad" does not require construction, but that the proper construction, if one is necessary is "a reference mark for cutting" (D.I. 135 at 24.)

CPT contends that the Court should construe "corner pad" as "a pad of metal or other conductive materials that is located at the corner of an outer guard ring, and electrically connected with the outer ring" (D.I. 137 at 15.) CPT argues, (Id.), and LPL does not dispute, that "corner pad" has no inherent meaning to one of ordinary skill in the art and thus can be understood only within the context of the '002 patent's claims and specification.

LPL does concede that "[o]ne of ordinary skill in the art would understand the term 'pad' to be a conductive area." (D.I. 135 at 15; D.I. 143 at 15.)

The term "corner pad" appears in only one embodiment in the specification. (See '002 patent, col. 8, ll. 1-48.) That embodiment describes three features of a "corner pad." First, it is connected to each other corner pad by conductive lines of the outer guard ring. (Id., col. 8, ll. 8-11.) Second, it can be grounded. (Id., col. 8, ll. 11-12.) Third, it provides

alignment for the scribe lines. (Id., col. 8, ll. 12-15.) The second feature is explicitly optional, so it need not be included in the Court's construction. The third feature is specifically claimed, so it too need not be included in the Court's construction. (See, e.g., Id., col. 9, ll. 29-33 ("7. The method as defined in claim 1 including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.")) Therefore, the Court concludes that LPL's proposed construction of "a reference mark for cutting" is unnecessary and would be redundant. The location of the corner pad is also specifically claimed as being "on at least one corner of the display." (See, e.g., Id., col. 9, l. 30.) Thus CPT's inclusion of "located at the corner of an outer guard ring" in its proposed construction is both unnecessary and inaccurate.

The remaining issue is whether the "corner pad" must be electrically connected to the outer guard ring. CPT bases its contention that the "corner pad" must be "electrically connected with the outer ring" on a single sentence from the specification: "A corner pad 208 is connected to each other corner pad (not illustrated) by respective outer conductive lines 210 and 212 of the guard ring 200." (Id., col. 8, ll. 8-11.) The Court concludes that it would be improper to import this limitation from the specification into the claims. Therefore, to the extent

that "corner pad" requires construction, the Court will construe it as "an area of conductive material."

F. Construction of "Pickup Pad"

LPL's proposed construction of "pickup pad" is "a conductive area used to electrically connect the back plane to the front plane" (D.I. 135 at 14.) CPT's proposed construction is "a pad located at the corner region of a backplane for aligning the frontplane and backplane" (D.I. 137 at 13.) CPT contends, and LPL does not dispute, that the term "pickup pad" has no inherent meaning to one of ordinary skill in the art, and thus, can be understood only within the context of the intrinsic evidence.

(D.I. 137 at 13.) The parties agree, however, that "pad" would be understood by one of ordinary skill in the art to mean a conductive area. (D.I. 135 at 15; D.I. 143 at 15; D.I. 160 at 3.) The Court concludes that neither proposed construction is appropriate and will decline to construe "pickup pad."

LPL's contention that the "pickup pad" is used to electrically connect the back plane to the front plane has no support in the intrinsic evidence. Neither the specification nor the claims of the '002 patent mentions any electrical connection between the front plane and the back plane via the "pickup pad". Both teach only the electrical connection of the "pickup pad" with other elements on the back plane. Thus, LPL's proposed construction cannot be correct.

CPT's proposed construction would violate the doctrine of claim differentiation. In this context, claim differentiation "refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim." Curtiss-Wright Control Corp. v. Velan, Inc., 438 F.3d 1374, 1380 (Fed. Cir. 2006) (citing Nazomi Communications, Inc. v. Arm Holdings, PLC., 403 F.3d 1364, 1370 (Fed. Cir. 2005)). In the '002 patent, claim 5 depends from claim 3.4 Claim 3 claims "[t]he method as defined in claim 2 including forming at least one pickup pad coupled to said resistance via a shunt switching element." ('002 patent, col. 9, ll. 16-18.) Claim 5 claims "[t]he method as defined in claim 3 including forming a corner on the said pad to align the front plane and back plane of the display." (Id., col. 9, 11. 23-25.) To construe "pickup pad" as CPT proposes, as "a pad . . . for aligning the frontplane and backplane," would be to read the limitation from claim 5 into claim 3, rendering claim 5 superfluous and violating the doctrine of claim differentiation.

All of the significant attributes of the "pickup pad" mentioned in the specification are also specifically claimed.

(Compare, '002 patent, col. 8, ll. 18-39, with id. col. 9, ll. 16-28.) Therefore, the Court concludes that no further

The discussion that follows applies identically to claims 16 and 14, 23 and 21, and 34 and 32.

construction of the term "pickup pad" is necessary.

CONCLUSION

An Order consistent with this Memorandum Opinion will be entered setting forth the meaning of the disputed terms and phrases in the '002 patent.

EXHIBIT L-2(c)

Filed 08/12/2008 Page 2 of 13 United States Patent [19] 4,820,222 Patent Number: [11] Holmberg et al. Date of Patent: Apr. 11, 1989 [45] METHOD OF MANUFACTURING FLAT 3,940,740 2/1976 Coontz 437/8 X PANEL BACKPLANES INCLUDING 4,368,523 1/1983 Kawate 358/236 X 4,586,242 5/1986 IMPROVED TESTING AND YIELDS Harrison 437/8 4,676,761 6/1987 Poujois 445/3 THEREOF AND DISPLAYS MADE 4,680,580 7/1987 Kawahara 340/784 **THEREBY** Primary Examiner—Kenneth J. Ramsey [75] Inventors: Scott H. Holmberg; Richard A. Attorney, Agent, or Firm-Silverman, Cass, Singer & Flasck, both of San Ramon, Calif. Winburn, Ltd. [73] Assignee: Alphasil, Inc., Fremont, Calif.

[21] Appl. No.: 948,224 [22] Filed: Dec. 31, 1986

[56]

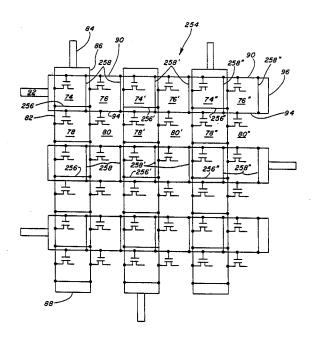
Int. Cl.⁴ G09G 3/22 [52] 445/24; 437/8

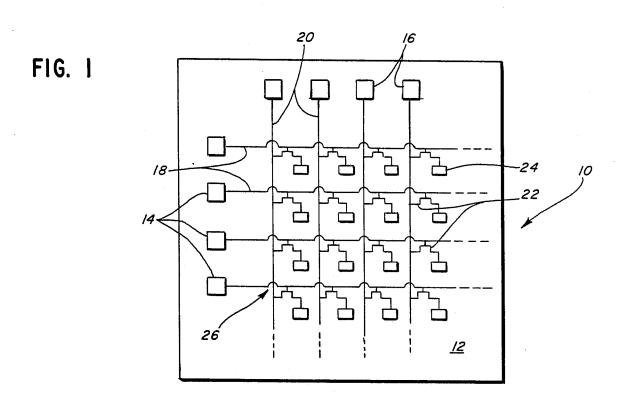
Field of Search 313/500; 340/784; 437/8; 445/3, 24, 25; 29/593 References Cited

U.S. PATENT DOCUMENTS 3,701,184 10/1972 Grier 445/24 ABSTRACT

Subdivided pixels are provided with interconnected and hence redundant row and column bus lines to reduce fatal defects. The respective redundant row and column lines also can be interconnected between subpixels to further reduce defects. One defective subpixel is generally an acceptable non-fatal defect, since the rest of the subpixels are still operative. The subpixels also can be formed with common row and column bus lines. The pixels or subpixels can be connected in a serial serpentine pattern to test all row or all column bus lines at once. After testing, the serial connections are broken.

31 Claims, 5 Drawing Sheets





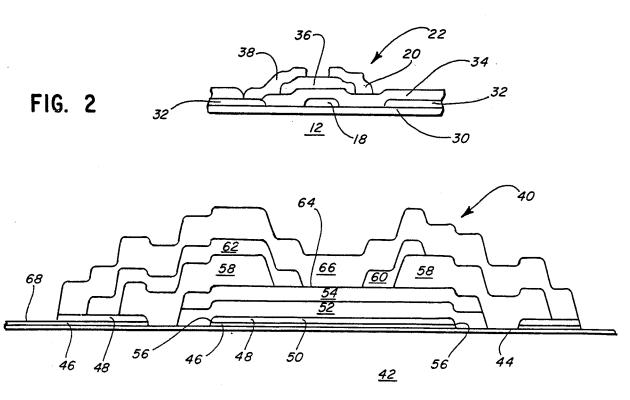
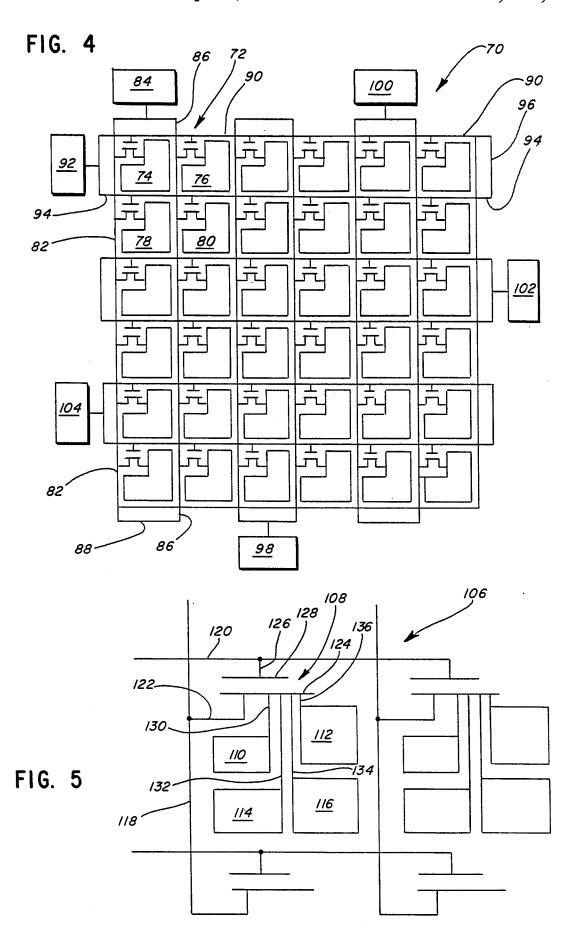
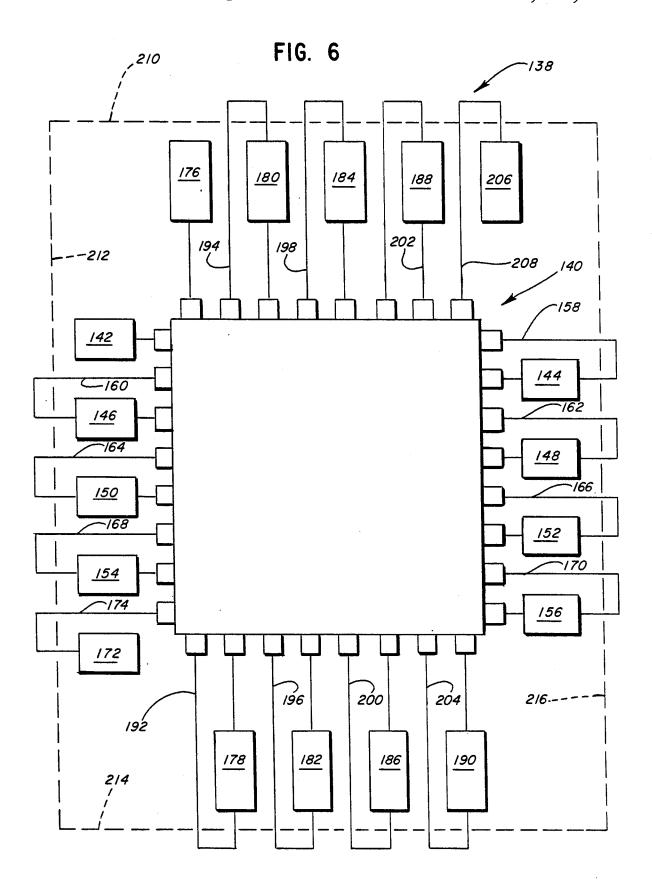
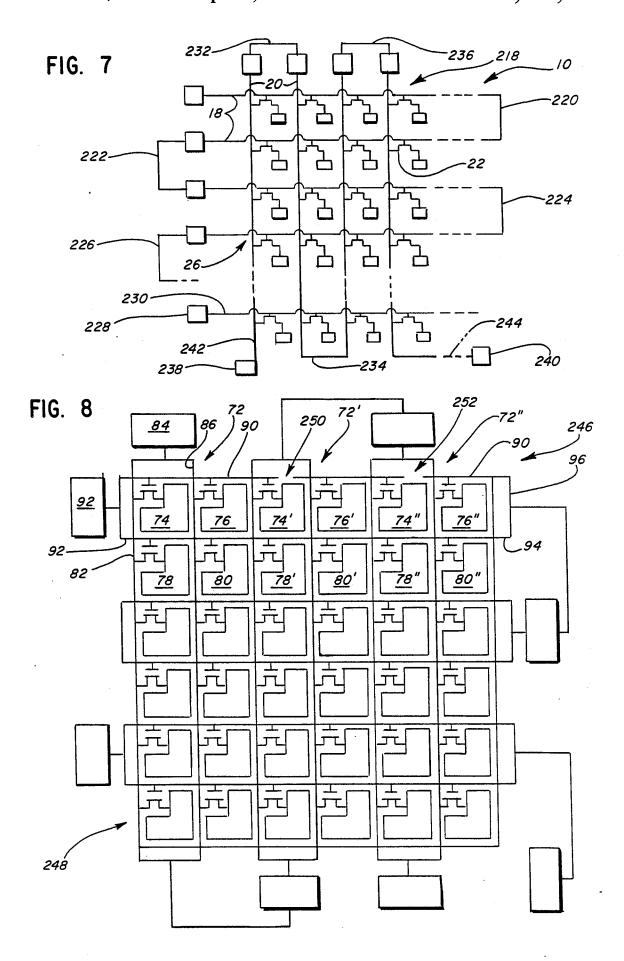


FIG. 3







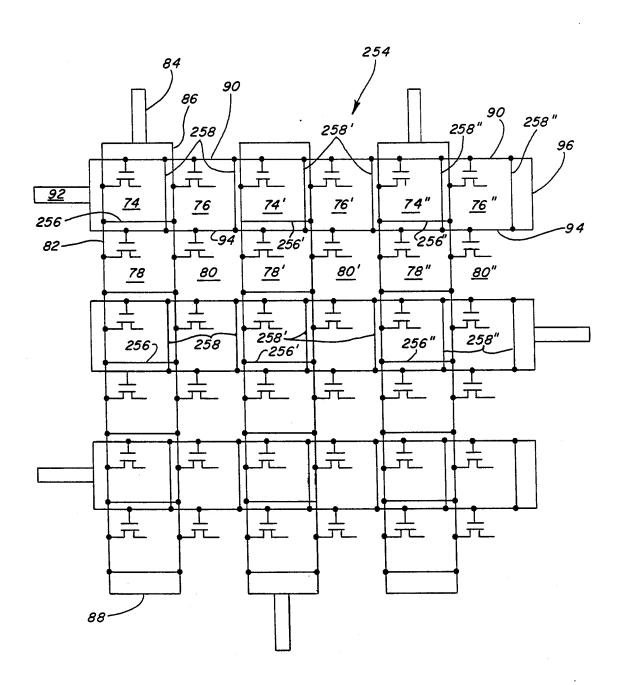


FIG. 9

1

METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING IMPROVED TESTING AND YIELDS THEREOF AND DISPLAYS MADE THEREBY

BACKGROUND OF THE INVENTION

The present invention pertains to improved flat panel displays and methods of making and testing the displays. More particularly, the present invention is di- 10 rected to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom.

In recent years there has been growing interest in flat panel displays, such as those which employ liquid crys- 15 tals, electrochromic or electroluminescence, as replacements for conventional cathode ray tubes (CRT). The flat panel displays promise lighter weight, less bulk and substantially lower power consumption than CRT's. Also, as a consequence of their mode of operation, CRT's nearly always suffer from some distortion. The CRT functions by projecting an electron beam onto a phosphor-coated screen. The beam will cause the spot on which it is focused to glow with an intensity proportional to the intensity of the beam. The display is cre- 25 ated by the constantly moving beam causing different spots on the screen to glow with different intensities. Because the electron beam travels a further distance from its stationary source to the edge of the screen than it does to the middle, the beam strikes various points on 30 the screen at different angles with resulting variation in spot size and shape (i.e. distortion).

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and 35 patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid 45 crystal, electroluminescent or electrochromic materials such as zinc sulfide, a gas plasma of, for example, neon and argon, a dichloroic dye, or such other appropriate material or device as will luminesce or otherwise of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

The circuitry for a flat panel display is generally 55 line. designed such that the flat panel timeshares, or multiplexes, digital circuits to feed signals to one row and column control line of the pixels at a time. Generally one driving circuit is used for each row or column control line. In this way a subthreshold voltage can be 60 interconnected in a serpentine fashion at the opposite fed to an entire row containing hundreds of thousands of pixels, keeping them all dark or inactive. Then a small additional voltage can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties. The pixels can be made to 65 glow brighter by applying a larger voltage or current of a longer pulse of voltage or current. Utilizing liquid crystal displays (LCD's) with twisted nematic active

material, the display is substantially transparent when not activated and becomes light absorbing when activated. Thus, the image is created on the display by sequentially activating the pixels, row by row, across the display. The geometric distortion described above with respect to CRT's is not a factor in flat panel displays since each pixel sees essentially the same voltage or current.

One of the major problems that arises with respect to the prior art method of manufacture of backplanes for active matrix displays (e.g. those employing thin film transistors at each pixel) is that they generally suffer production yield problems similar to those of integrated circuits. That is, the yields of backplanes produced are generally not 100% and the yield (percentage of backplanes with no defects) can be 0% in a worst case. High quality displays will not tolerate any defective pixel transistors or other components. Also, larger size displays are generally more desirable than smaller size displays. Thus, a manufacturer is faced with the dilemma of preferring to manufacture larger displays, but having to discard the entire product if even one pixel is defective. In other words, the manufacturer suffers a radically increased manufacturing cost per unit resulting from decreasing usable product yield.

These problems of increased cost and decreased yield are dramatically improved in the present invention by providing methods of manufacturing display backplanes and the resulting displays with a greatly reduced number of fatal defects.

SUMMARY OF THE INVENTION

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to greatly increase the manufacturing yield, decrease manufacturing costs and decrease the number of fatal display defects.

These improvements are accomplished by subdividwith a pixel contact and control element between the 40 ing each of the backplanes and hence display pixels into two or more subpixels. Each subpixel is formed with its own row (gate) line and column (source) bus line. Each subpixel pair of bus row lines and each pair of bus column lines are connected at the opposite sides of the display to provide redundant bus row lines and bus column lines. A break in the row or column bus line therefore will not affect the operation of the display, because the pixel will receive current from the other interconnected end of the row or column bus line Furchange optical properties in response to the application 50 ther, by providing subpixels, a defective active device at a subpixel will result in less than the whole pixel being defective and hence can be an acceptable nonfatal defect increasing the display yields. Subpixels also can be formed with a common row and a common column bus

The cost of manufacturing the display backplanes and hence the displays also can be reduced by serial loop testing of the row and column bus lines during manufacture. Each of the row and column bus lines is serially edges of the display. This allows all the row and all the column bus lines to be tested merely by contacting the two free ends of each of the serially interconnected row and column bus lines. Further, by applying the proper voltage to the ends of both the row and column bus lines, all the pixels or subpixels will be activated to provide one whole display test of all the pixels or subpixels at once. After final testing, the row and bus col-

umn line interconnections are broken to complete the display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view schematic representation of an 5 active matrix display backplane made by a prior art method;

FIG. 2 is a cross-section of one transistor of the prior art backplane which could be utilized with the present

FIG. 3 is a cross-section of one transistor which could be utilized with the present invention;

FIG. 4 is a plan view schematic representation of one embodiment of a subpixel matrix display of the present

FIG. 5 is a plan view schematic representation of another embodiment of a subpixel matrix display of the present invention;

FIG. 6 is a plan view schematic representation of one embodiment of serial serpentine testing of the subpixel 20 carded. row and column bus lines in accordance with the pres-

FIG. 7 is a plan schematic view of serial serpentine testing of conventional row and column bus lines in accordance with the present invention:

FIG. 8 is a plan view schematic of the subpixel matrix display of FIG. 4 with several row and column bus line defects or breaks therein; and

FIG. 9 is a plan view schematic of a subpixel matrix display of the invention similar to FIG. 8 with row and 30 column bus line interconnections to avoid fatal defects caused by greater than one break in a particular row or bus column line.

DESCRIPTION OF THE PREFERRED **EMBODIMENTS**

Referring now more particularly to FIG. 1, there is shown a schematic representation of an active matrix flat panel display device 10 made in accordance with conventional photolithographic techniques. One such 40 device 10 and the manufacture thereof is more fully described in Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels, A. J. Snell, et al., Applied Physics, No. 24, p. 357, 1981. The device 10 includes a substrate 12, sets of 45 18 very thin, but the resistivity is then too high to make contact pads 14 and 16, sets of control or bus lines 18 and 20, and, in this particular example of the prior art, transistors 22 and pixel back contacts 24.

The substrate 12 commonly employed in these devices is formed from glass. The control lines 18 and 20 50 are organized into a matrix of rows 18 and columns 20. The control line rows 18 in this device 10 serve as gate electrodes and the control line columns 20 as source connections. One contact pad 14 is connected to one end of each of the row control lines 18. One contact pad 55 16 is connected to one end of each of the column control lines 20. The display drive control (not shown) is connected to the sets of pads 14 and 16.

At each matrix crossover point 26, where a row line 18 and a column line 20 cross, a switching element, 60 transistor 22 is formed to connect the row line 18 and column line 20 to the pixel back contacts 24. The active medium is deposited at least on the contacts 24 which will optically change properties in response to the compoint 26 formed by the row 18 and column 20. The active medium at a given crossover point 26 will appear as a square or dot in the overall checkerboard type

matrix of the display 10. The actual size of the transistors 22 and the contacts 24 are not now drawn to scale. but are shown schematically for illustration only.

It should be noted that theoretically there is no limit on the number of rows 18 and columns 20 that can be employed, only a portion of which are illustrated in FIG. 1. Therefore, there is also no theoretical limit on the outside dimensions of such a device 10. However, the present state of the lithographic art places a practical limit on the outside dimensions of these devices. The present alignment techniques generally allow high resolution display devices to be manufactured approximately five inches on a side 28, although improved techniques of up to fourteen inches on a side has been 15 demonstrated.

The problem encountered by the prior art method of manufacture is that if the array of device 10 contains any defective pixel transistors 22 or other circuit elements causing a pixel to be inoperative, it must be dis-

Referring in detail to FIG. 2, several problems occur when the switching element, transistor 22 is manufactured. The substrate 12 is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid crystal display manufacturers that the high sodium concentration can poison the liquid crystal material by diffusing through the overlying ITO layer and hence an SiO₂ suppression layer 30 is generally formed on the substrate 12. There are some high quality low sodium types of substrates available, which would not need the suppression layer 30. An ITO layer 32 is formed and etched to provide an ITO free area on which the gate 18 is deposited. Following the deposition of the gate 18, a 35 gate insulator layer 34 is deposited. Although a smooth uniform coverage of the gate 18 by the insulator 34 is illustrated, in production the gate 18 has or can have sharp edges which lead to pin holes or thinning of the insulator 34 at the gate edges. The source and drain metals can short to the gate 18. The thinning or pin holes produce transistors 22, which if operative, do not have uniform operating characteristics and hence the backplane is worthless.

One attempt to solve this problem, is to make the gate the large arrays necessary for the backplane. A second attempt to solve the problem is to make the gate insulator 34 very thick, but this decreases the gain of the transistor 22 and is also self defeating.

An amorphous silicon layer 36 is then deposited, with the source 20 and a drain 38 deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor 22. During operation the activation of the source 20 and the gate 18 couples power through the silicon alloy 36 to the drain and hence to the contact pad 24 formed by the ITO layer 32.

Referring now to FIG. 3, there is shown a schematic representation of one embodiment of a transistor 40 which can be utilized with the present invention. The transistor is more fully disclosed in U.S. Pat. No. 4,545,112 and U.S. Ser. No. 493,523, which are incorporated herein by reference.

A glass substrate 42 includes a barrier SiO2 layer 44 bined voltages or currents in the respective crossover 65 thereon. As above mentioned, a low sodium glass substrate, such as Corning 7059 glass, could be utilized, and hence the barrier layer 44 can be eliminated The detailed deposition steps are described in the above-

referenced patent and application. An ITO layer 46 is deposited and then a refractory metal layer 48 is deposited on the ITO layer 46.

The layers 46 and 48 are etched to form a gate electrode 50. A gate insulator 52 and a semiconductor mate- 5 rial 54 are sequentially deposited over the gate 50. The material 54 preferably is an amorphous silicon alloy. To avoid the possibility of any gate to source or drain shorts at gate edges 56, a dielectric 58 is deposited over the gate 55, the gate insulator 52 and the semiconductor 10 54. The dielectric 58 is deposited to a sufficient thickness to ensure that no shorts or thin spots are formed between the edges 56 of the gate 50 and a source 60 and a drain 62 deposited thereover.

The dielectric 58 is etched away only on a substantially planar central region 64 of the semiconductor layer 54. This insures uniform operating characteristics for the transistors 40 in the backplane array. A passivating layer 66 is deposited over the whole structure to complete the structure of the transistor 40.

During all of the transistor processing steps, the refractory metal layer 48 remains over a pixel contact pad 68 upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad 68 leaving the ITO layer 46 exposed after all the processing has been completed.

Referring now to FIG. 4, a subpixel matrix display of 30 the present invention is designated generally by the reference numeral 70. The subpixel matrix display 70 is illustrated as having each pixel subdivided into four subpixels, but the pixels could be subdivided into nuby four or six subpixels or in three subpixels for color applications. Each pixel 72 is subdivided into four subpixels 74, 76, 78 and 80 (only one pixel 72 is so numbered for illustration). As previously stated, the number the display 70 could contain any desired number and configuration, square or rectangular.

A column (source) line or bus 82 connects the subpixels 74 and 78 and all other column subpixel pairs in one-half of each of the pixels to a column or source 45 contact pad 84 at one edge of the display 70. A second column (source) line or bus 86 connects the subpixels 76 and 80 and all other column subpixel pairs in the second half of each of the pixels to the column or source nected (shorted) at or before the pad 84 and are interconnected (shorted) at the opposite ends by a line or short 88.

A row (gate) line or bus 90 connects the subpixels 74 and 76 and all other row subpixel pairs in one-half of 55 each of the pixels to a row (gate) pad 92. A second row (gate) line or bus 94 connects the subpixels 78 and 80 and all other row subpixel pairs in one-half of each of the pixels to the row pad 92. The bus lines 90 and 94 are interconnected (shorted) at or before the pad 92 and are 60 interconnected (shorted) at the opposite ends by a line or short 96.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) trated as being on opposite sides of the display to provide additional connecting space for the pads, however, they also could all be on one side as in the display 10.

Each of the other subpixel pairs also are connected in rows to respective row (gate) pads 102 and 104, etc.

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The pixel 72 then is divided into four subpixels 74, 76 78 and 80 which allows for one of the subpixels to be defective, such as the subpixel 74, without causing a fatal defect, since the remaining three subpixels 76, 78 and 80 remain operative. In prior devices, the pixel 72 would be totally defective and hence the display 70 would be inoperable.

Further, one often fatal display defect is caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display 70. With the respective subpixel pairs of row and column bus lines interconnected, however, an open in a bus line will at most cause one subpixel to be inoperative. An open in one or more of the bus lines between the subpixels will result in no defects, since the current is supplied from the opposite shorted end of the row or column bus line. Thus, the display 70 in effect has redundant row and column bus lines.

Referring to FIG. 5, a second embodiment of a subpixel matrix display of the present invention is designated generally by the reference numeral 106. Again, a pixel 108 is subdivided into a plurality of subpixels 110, 112, 114 and 116. In this embodiment, each of the subpixels 110, 112, 114 and 116 has a common column (source) line or bus 118 and a common row (gate) line or bus 120. The column bus line 118 is coupled by a source line 122 to a line 124, which is a schematic representation of a common source electrode. The row bus line 120 is coupled (schematically) by a line 126 to a line 128 which is a schematic representation of a gate elecmerous other configurations such as two subpixels, two 35 trode. Each of the subpixels 110, 112, 114 and 116 is coupled by a separate respective drain line 130 132, 134 and 136 to the (schematic) common source electrode 124. Since the drain lines 130, 132, 134 and 136 are small and formed close to one another to utilize the least of pixels is merely shown for illustration purposes and 40 space, a short in one of the lines, such as the drain line 130 causes only the subpixel 110 to be defective.

A flat panel backplane testing configuration is generally designated by the numeral 138 in FIG. 6. A flat panel backplane configuration 140 having subpixels similar to the display 70 of FIG. 4 includes a plurality of interconnected row (gate) lines or buses which are connected as described above to a plurality of row (gate) pads 142, 144, 146, 148, 150, 152, 154 and 156.

Additionally, each of the row pads 142, 144, 146, 148, contact pad 84. The bus lines 82 and 86 are intercon- 50 150, 152, 154 and 156 and hence each of the row (gate) lines or buses is interconnected in a serpentine fashion by respective lines or shorts 158, 160, 162, 164, 166, 168 and 170. In addition, to allow the testing of the last pair of row lines from the row pad 156, an additional or test row pad 172 is added to the test configuration 138, which is coupled to the last pair of row bus lines by a line 174.

Each of a pair of a plurality of interconnected column (source) lines or buses is connected to a respective column (source) pad 176, 178, 180, 182, 184 186 188 and 190 as described above. As with the row bus lines and pads, each column pad 176, 178, 180, 182, 184, 186, 188 and 190 is interconnected in a serpentine fashion by respective lines or shorts 192, 194, 196, 198, 200, 202 and pads 98 and 100, etc. The pads 84, 98 and 100 are illus- 65 204. Again, to test the last pair of column bus lines, an additional or test column pad 206 is added to the test configuration 138, which is coupled to the last pair of column bus lines by a line 208.

As soon as the row bus lines (presuming the row bus lines are deposited first) are formed, all of the row bus lines can be tested merely by contacting two test points, the pads 142 and 172. In a like manner, the column bus lines can be tested simultaneously by contacting the two 5 pads 176 and 206. The tests can be repeated as desired during the manufacturing process and appropriate repairs or termination of the manufacturing process can occur to reduce the manufacturing costs and to increase the yield of the completed display.

If the display is an inactive matrix without transistors or other active devices, then once the row and column bus lines have been tested as having continuity, then the serpentine interconnections are opened or broken to complete or allow completion of the display backplane. 15 Preferably, especially where the devices are formed on glass, the interconnecting lines 158, 160, etc. and 192, 194, etc. extend beyond their respective pads, such that four scribe lines 210, 212, 214 and 216 intersecting all of the connecting lines can be formed. The glass substrate 20 then is broken off along each of the scribe lines 210 212, 214 and 216 to terminate the test interconnections.

Where the subpixel display device 140 includes active devices, such as the transistors previously described, then the transistors also will be tested prior to terminat- 25 ing the interconnections. Further, if desired, the liquid crystal medium can be added and the whole display can be tested at once to see if all the pixels of the whole display 140 are operable prior to terminating the connections. In this case, one or both row pads 142 and 172 30 are contacted with an appropriate row or gate activation voltage.

In a like manner, one or both column pads 176 and 206 are contacted with an appropriate column or source activation voltage. Also, the backplane contact (not 35 illustrated) is contacted with an appropriate activation voltage, which will activate all of the pixels for a visual test of the display device 140

Referring to FIG. 7, the prior art device 10 (FIG. 1) is illustrated having a test configuration 218. The row 40 bus lines 18 are interconnected in a serpentine fashion by a plurality of connecting lines 220, 222, 224 and 226 (partially shown). Depending upon the number of bus lines, the device 10 may not need an additional test pad, since the device ends in a pad 228 on the last row bus 45 line 230. In a like manner, the column bus lines are interconnected in a serpentine fashion by a plurality of connecting lines 232, 234 and 236. If desired, or the configuration requires, a pair of column test pads 238 and 240 with respective connecting lines 242 and 244 50 are utilized to test the display 10 as described with respect to FIG. 6, prior to terminating or removing the connecting lines. Generally, the device 10 would be configured with the column pads all on the same side as illustrated for the row pads.

Referring to FIG. 8, a test configuration 246 with a subpixel display 248 is best illustrated, which is similar to the display 70 of FIG. 4, with the serpentine test configuration of FIG. 6. Like numerals for the like parts from those described in FIG. 4, are utilized where ap- 60 propriate. As described before, the redundant row bus lines 90 and 94 will provide the operating current to all the subpixels 74, 76, 74', 76', etc. if a single break or defect 250 occurs in one of the lines 90. In that case the from the pad 92 on one end of the bus line 90, while the subpixels 76', 74" and 76" are fed via the pad 92, the bus line 94 across the short 96 and via the other end of the

bus line 90. If, however, a second break 252 occurs in the same bus line 90, then no current will be fed to the subpixels 76' and 74", which then are isolated. Two or more adjacent subpixels being inoperative generally

would be a fatal defect and the redundant row bus lines 90 and 94 then would not be sufficient to save the display 248. In a like manner, two or more breaks in any of the row or column bus lines or pairs of bus lines gener-

ally will render the display inoperative.

To avoid the fatal defect of the multiple open lines another redundant display configuration is designated generally by the numeral 254 in FIG. 9. The redundant row and column bus lines are further interconnected in the display 254 at each subpixel to avoid the fatal defect illustrated in FIG. 8.

The display 254 is illustrated only with the bus line and interconnection patterns without the subpixels for clarity. Each pair of the column bus lines 82 and 86 are additionally interconnected between each of the subpixels 74, 78, etc. by respective lines or shorts 256, 256' and 256". In a like manner, each pair of the row bus lines 90 and 94 are interconnected between each of the subpixels 74, 76, etc. by respective lines or shorts 258.

With the additional interconnections 256 and 258, the previously fatal double open defects 250 and 252 do not cause the loss of any subpixels. The subpixels 76' and 74" now are fed via the bus line 94 and the short connecting line 258'. Therefore, the display 254 does not have any subpixel defects. Further, although both the row bus lines and the column bus lines have been illustrated as being interconnected between each subpixel, only one of the row or the column bus line sets might be shorted to limit the loss of active pixel display area.

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A method of manufacturing matrix display backplanes and displays therefrom, comprising: providing a substrate;

providing a pattern of pixels on said substrate; and providing a plurality of sets of intersecting pixel acti-

vation bus lines and coupling each said pixel to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines, including connecting each of said pixels to one of its redundant pair of activation bus lines and interconnecting each end of said redundant pair of activation bus lines to one another to provide said redundancy and dividing each pixel into a plurality of subpixels and connecting each of said subpixels to one of its redundant pair of activation bus lines through an active device, independent of any other pixel activation bus lines.

- 2. The method as defined in claim 1 including interrow bus lines for the subpixels 74, 76 and 74' are fed 65 connecting each of said redundant pair of activation bus lines between each of said pixels.
 - 3. The method as defined in claim 1 including providing a redundant pair of row activation bus lines and a

redundant pair of column activation bus lines for each of said pixels.

- 4. The method as defined in claim 3 including interconnecting at least one pair of said row and column lines between each of said pixels.
 - 5. A display having dual bus lines, comprising: a substrate;
 - a pattern of pixels formed on said substrate; and
 - a plurality of sets on intersecting pixel activation bus lines formed on said substrate and each said pixel 10 coupled to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines, including each of said pixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to one another to provide said redundancy and each pixel divided into a plurality of subpixels and each of said subpixels connected to one of its redundant pair of activation bus lines through an active device, indepen-20 dent of any other pixel activation bus lines.
- 6. The display as defined in claim 5 including each of said redundant pair of activation bus lines interconnected between each of said pixels.
- 7. The display as defined in claim 5 including a redundant pair of row activation bus lines and a redundant pair of column activation bus lines connected to each of said pixels.
- 8. The display as defined in claim 7 including at least 30 one pair of said row and column lines interconnected between each of said pixels.
- 9. A method of manufacturing matrix display backplanes and displays therefrom, comprising:

providing a substrate;

providing a pattern of pixels on said substrate;

providing a plurality of sets of intersecting pixel activation bus lines and coupling each said pixel to at least one of said sets of intersecting bus lines to provide each pixel with a set of activation bus lines; 40

forming said activation bus lines substantially orthogonal to one another in a plurality of rows and a plurality of columns of bus lines;

interconnecting opposite ends of each of said plurality of row bus lines in a serpentine fashion to seri- 45 ally connect substantially all of said row bus lines to one another;

interconnecting opposite ends of each of said plurality of column bus lines in a serpentine fashion to serially connect substantially all of said column bus 50 lines to one another;

testing the continuity of substantially all of said plurality of row and column bus lines by contacting only two test points on each of said interconnected row and column bus lines as the backplanes are 55 planes and displays therefrom, comprising: being manufactured; and

terminating substantially all of said interconnections after said bus lines are tested as having continuity to complete the manufacture of the backplanes and displays therefrom.

10. The method as defined in claim 9 including providing a plurality of sets of intersecting pixel activation bus lines and coupling each said pixel to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines and intercon- 65 necting opposite ends of each respective pair of said plurality of row and column bus lines to test the continuity of said sets of row and column bus lines.

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- 11. The method as defined in claim 10 including connecting each of said pixels to one of its redundant pair of activation bus lines and interconnecting each end of said redundant pair of activation bus lines to one another to provide said redundancy.
- 12. The method as defined in claim 11 including dividing each pixel into a plurality of subpixels and connecting each of said subpixels to one of its redundant pair of activation bus lines.
- 13. The method as defined in claim 12 including interconnecting at least one pair of said row and column lines between each of said pixels.
- 14. A display backplane having interconnections, comprising
 - a substrate;
 - a pattern of pixels formed on said substrate;
 - a plurality of sets if intersecting pixel activation lines formed on said substrate and each said pixel coupled to at least one of said sets of intersecting lines by an active device to provide each pixel with a set of activation lines;
 - said activation lines formed substantially orthogonal to one another in a plurality of rows and a plurality of columns of lines;
- opposite ends of each of said plurality of row lines interconnected in a serpentine fashion to serially connect substantially all of said row lines to one another:
- opposite ends of each of said plurality of column bus lines interconnected in a serpentine fashion to serially connect substantially all of said column bus lines to one another; and
- a pair of test points on each of said row and said column bus lines.
- 15. The backplane as defined in claim 14 including a plurality of sets of intersecting pixel activation bus lines, each said pixel coupled to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines and opposite ends of each respective pair of said plurality of row and column bus lines interconnected.
- 16. The backplane as defined in claim 15 including each of said pixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to one another to provide said redundancy.
- 17. The backplane as defined in claim 16 including each pixel divided into a plurality of subpixels and each of said subpixels connected by an active device to one of its redundant pair of activation bus lines.
- 18. The backplane as defined in claim 17 including at least one pair of said row and column lines interconnected between each of said pixels.
- 19. A method of manufacturing matrix display back-

providing a substrate;

providing a pattern of pixels on said substrate; subdividing each of said pixels into at least two sub-

pixels: and

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providing a plurality of sets of intersecting subpixel activation bus lines and coupling each said subpixel to at least one of said sets of intersecting bus lines to provide each subpixel with a set of activation bus lines through an active device, independent of any other pixel activation bus lines.

20. The method as defined in claim 19 including connecting each of said subpixels to one of its redundant pair of activation bus lines and interconnecting each end

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of said redundant pair of activation bus lines to one another to provide said redundancy.

21. The method as defined in claim 20 including interconnecting each of said redundant pair of activation bus lines between each of said subpixels.

22. The method as defined in claim 24 including interconnecting opposite ends of each of said plurality of row bus lines in a serpentine fashion to serially connect substantially all of said row bus lines to one another;

interconnecting opposite ends of each of said plurality of column bus lines in a serpentine fashion to serially connect substantially all of said column bus lines to one another:

testing the continuity of substantially all of said plurality of row and column bus lines by contacting 15 only two test points on each of said interconnected row and column bus lines as the backplanes are being manufactured; and

terminating substantially all of said interconnections after said bus lines are tested as having continuity 20 to complete the manufacture of the backplanes and displays therefrom.

23. The method as defined in claim 22 including testing all of said subpixels by contacting said two row and said two column bus line test points.

24. The method as defined in claim 19 including providing a redundant pair of row activation bus lines and a redundant pair of column activation bus lines for each of said subpixels.

25. The method as defined in claim 24 including inter-30 connecting at least one pair of said row and column lines between each of said subpixels.

26. A display backplane having subpixels, comprising:

a substrate;

a pattern of pixels formed on said substrate; each of said pixels subdivided into at least two subpix-

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eis; an

a plurality of sets of intersecting pixel activation bus lines formed on said substrate and each said subpixel coupled to at least one of said sets of intersecting bus lines to provide each subpixel with a set of activation bus lines through an active device, independent of any other pixel activation bus lines.

27. The display as defined in claim 26 including each of said subpixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to on another

5 to provide said redundancy.

28. The display as defined in claim 27 including each of said redundant pair of activation bus lines interconnected between each of said subminels.

nected between each of said subpixels.

29. The display as defined in claim 27 including opposite ends of each of said plurality of row bus lines interconnected in a serpentine fashion to serially connect substantially all of said row bus lines to one another; and opposite ends of each of said plurality of column bus

lines interconnected in a serpentine fashion to serially connect substantially all of said column bus

lines to one another.

30. The display as defined in claim 26 including a redundant pair of row activation bus lines and a redundant pair of column activation bus lines connected to each of said subpixels.

31. The display as defined in claim 30 including at least one pair of said row and column lines interconnected between each of said subpixels.

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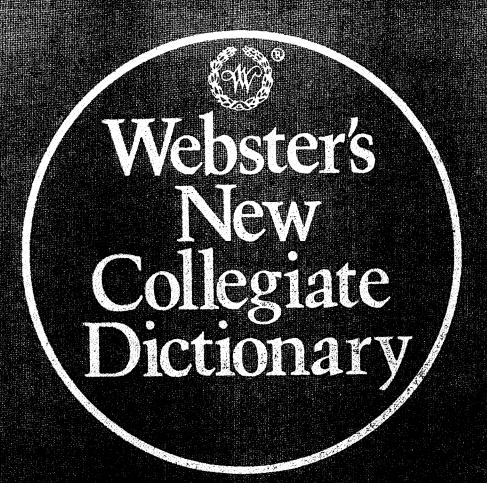
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EXHIBIT L-2(d)



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Library of Congress Cataloging in Publication Data Main entry under title:

Webster's new collegiate dictionary.

Editions for 1898-1948 have title: Webster's collegiate dictionary. Includes index.

1. English language—Dictionaries.
PE1628.W4M4 1980 423 79-24073
ISBN 0-87779-398-0
ISBN 0-87779-399-9 (indexed)
ISBN 0-87779-400-6 (deluxe)

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Made in the United States of America

3536373839RMcN80

reserved power n: a political power reserved by a constitution to the exclusive jurisdiction of a specified political authority reserve price n: a price announced at an auction as the lowest that will be considered

reservoir \frac{1}{re-server} n: a member of a military reserve

reservoir \frac{1}{rez-o(r)v_war, -o(r)v_v(w) or also -o(r)_voi\ n [F reservoir, fr. MF, fr. reserver]

1: a place where something is kept in

store: as a: an artificial lake where water is collected and kept in store: as a: an artificial lake where water is collected and kept in quantity for use b: a part of an apparatus in which a liquid is held c: SUPPLY. STORE (a large ~ of educated people) 2: an extra supply: RESERVE 3: an organism in which a parasite that is pathogenic for some other species lives and multiples without damaging its host; also: a noneconomic organism within which a pathogen of economic or medical importance flourishes reset \('\)res'est\ vt .set: set-ting 1: to set again or anew \(\times \) type\ \(\times \) a diamond\ 2: to change the reading of \(\times \) an odometer\(\times \) reset-table \(\times \) set-bol\(adi \) res ges-tae \(\times \) tigs-'ges-tif, 'rez-'jes-(\)te\ \(n \) pl [L]: things done; esp: the facts that form the environment of a litigated issue and are admissible in evidence

admissible in evidence

resh \'rash\ n [Heb resh]: the 20th letter of the Hebrew alphabet - see ALPHABET table

reshape (')re'shap\ vt: to give a new form or orientation to

REORGANIZE - reshaper n

Reorganize - reshaper n

reship \(')re-'ship\ vi: to ship again; specif: to put on board a second time $\sim vi$: to embark on a ship again or anew; specif: to sign again for service on a ship — re-ship-ment \-mant\ n — re-

re-shuf-fle \(')re-'shaf-al\ vt 1: to shuffle (as cards) again 2: to

re-shuf-fle \(')r\tilde{c}\shot-ol\ vt 1: to shuffle (as cards) again 2: to reorganize usu. by the redistribution of existing elements (the cabinet was reshuffled by the prime minister)— reshuffle n re-sid\('\)n': RESIDUAL OIL
re-side \('\)ri-'zid\ vi re-sid-ed; re-sid-ing [ME residen, fr. MF or L; MF resider, fr. L residere to sit back, remain, abide, fr. re- + sed\('\)re-to sit — more at SIT] 1 a: to be in residence as the incumbent of a benefice or office b: to dwell permanently or continuously: occupy a place as one's legal domicile 2 a: to be present as an element or quality b: to be vested as a right — re-sid-er n
syn RESIDE, LIVE, DWELL, SOJOURN shared meaning element: to have as one's habitation or domicile

element or quality b: to be vested as a right — re-sider n
syn RESIDE, LIVE, DWELL, SOJOURN shared meaning element: to
have as one's habitation or domicile
res-i-dence \(\) 'rez-ad-an(t)s, 'rez-don(t)s, 'rez-a-,den(t)s\\ n 1 a
: the act or fact of dwelling in a place for some time b: the act or
fact of living or regularly staying at or in some place for the discharge of a duty or the enjoyment of a benefit 2 a (1): the
place where one actually lives as distinguished from his domicile
a place of temporary sojourn (2): DOMICILE 2a b: the place
where a corporation is actually or officially established c: the
status of a legal resident 3 a: a building used as a home
the status of a legal resident 3 a: a building used as a home
the status of a legal resident and the status of a legal resident control of abode in a place (after a \(\) of 30
years\(\) b: housing or a unit of housing provided for students

4 a: the period or duration of abode in a place (after a \(\) of 30
years\(\) b: a period of active and esp. full-time study, research, or
teaching at a college or university 5: the persistence of a substance that is suspended or dissolved in a medium (the \(\) time of a
pollutant\(\) — in residence: engaged to live and work at a particular place often for a specified time (poet in residence at a university)

residence \(\) \(\) \(\) rez-ad-an-s\(\), 'rez-a-d-an, 'rez-a-,den(t)-\(\) \(n, p \) -cies 1
: a usu. Official place of residence 2: a territory in a protected
state in which the powers of the protecting state are executed by a
resident agent 3: a period of advanced training in a medical
specialty

residing at a foreign court or seat of government; esp: one exercising authority in a protected state as representative of the protecting power 3: a physician serving a residency

resident commissioner n 1: a nonvoting representative of a dependency in the U.S. House of Representatives 2: a resident administrator in a British colony or possession

residential _irez(-3)-'den-chal\ adj 1 a: used as a residence or by residents b: providing living accommodations for students (a \sim \colon \colon \colon college) 2: restricted to or occupied by residences (a \sim \colon \co

distillates (as gasoline) from petroleum and that is used esp. by industry — called also resid

residual power n: power held to remain at the disposal of a governmental authority after an enumeration or delegation of specified powers to other authorities

re-sid-u-ary \ri-'zij-a-, wer-e\ adj: of, relating to, or constituting a

residue \rez-2-,d(y)\(\times\) | [ME, fr. MF residu, fr. L residuum, fr. neut. of residuus left over, fr. residere to remain]: something that remains after a part is taken, separated, or designated: REMNANT. REMAINDER: as a: the part of a testator's estate remaining after the satisfaction of all debts, charges, allowances, and previous devises and bequests b: the remainder after subtracting a multiple of a modulus from an integer or a power of the integer: the second of two terms in a congruence (2 and 7 are ~s of 12 modulo 5) (9 is a quadratic ~ of 7 modulo 5 since $7^2 - 8 \times 5 = 9$) c: a constituent structural unit (as a group or monomer) of a usu. complex molecule (amino acid ~s left after hydrolysis of protein) residue class n: the set of elements (as integers) that leave the same remainder when divided by the same modulus residua unitariation of personal a complex a b: a residual product (as from the distillation of petroleum) resign of petroleum) resign of petroleum)

distillation of petroleum)

resign \ri-'zin\ vb [ME resignen, fr. MF resigner, fr. L resignare, lit.,
to unseal, cancel, fr. re- + signare to sign, seal — more at SIGN] vt

1: to give up deliberately; esp: to renounce (as a right or position) by a formal act 2: RELEGATE, CONSIGN; esp: to give (oneself) over without resistance (~ed herself to her fate) ~ vi 1: to give up one's office or position: QUIT 2: to accept something as inevitable: SUBMIT syn see RELINQUISH, ABDICATE — re-sign-ed-ly \-'zi-nad-l\bar{e}\ adv — re-sign-ed-ness \-'zi-nad-nas\ n — re-sign-er

resignation \rez-ig-'nā-shon\ n 1 a : an act or instance of resigning something : SURRENDER b : a formal notification of resigning 2 : the quality or state of being resigned : SUBMISSIVE-

re-sile \ri-'zī(ə)l\ vi re-siled; re-sil-ing [LL & L; LL resilire to with-draw, fr. L, to recoil]: RECOIL, RETRACT; esp: to return to a prior

re-sil-ience \ri-'zil-yon(t)s\ n 1: the capability of a strained body to recover its size and shape after deformation caused esp. by compressive stress 2: an ability to recover from or adjust easily to misfortune or change

misfortune or change
re-sil-ien-cy\-y-y-se\n: RESILIENCE
re-sil-ient\-y-y-nt\ adj [L resilient-, resiliens, prp. of resilire to jump
back, recoil, fr. re- + salire to leap — more at SALLY]: characterized or marked by resilience: as a: capable of withstanding shock
without permanent deformation or rupture b: tending to recover
from or adjust easily to misfortune or change — re-sil-ient-ly adv
'res-in\rez-'n\ n [ME, fr. MF resine, fr. L resina, fr. Gk rhētine
pine resin] 1 a: any of various solid or semisolid amorphous
tusible flammable natural organic substances that are usu. transparent or translucent and yellowish to brown, are formed esp. in
plant secretions, are soluble in organic solvents (as ether) but not
in water, are electrical nonconductors, and are used chiefly in var-

in water, are electrical nonconductors, and are used chiefly in varin water, are electrical nonconductors, and are used chiefly in varnishes, printing inks, plastics, and sizes and in medicine **b**: Rosil **2 a**: any of a large class of synthetic products that have some of the physical properties of natural resins but are different chemically and are used chiefly as plastics **b**: any of various products made from a natural resin or a natural polymer ²resin vt res-ined; res-in-ing \'rez-²n-in, 'rez-nin\': to treat with resin

res-in-ate \'rez-on-at\ vt -at-ed; -at-ing : to impregnate or flavor with resin

resin canal n: a tubular intercellular space in gymnosperms and some angiosperms that is lined with epithelial cells which secrete resin — called also resin duct

re-sin-i-fy \re-'zin-a-ifi\ vt -fied; fy-ing : to convert into or treat

with resin resin-oid \resin-oid \ n 1 a: a somewhat resinous substance b: a thermosetting synthetic resin 2: GUM RESIN resin-ous \rez-nos. 3 n-os\ adj: of, relating to, resembling, containing, or derived from resin resist \ri-zist\ vb [ME resisten, fr. MF or L; MF resister, fr. L resistere, fr. re- + sistere to take a stand; akin to L stare to stand — more at STAND] vt 1: to withstand the force or effect of 2: to exert force in exert oneself so as to counteract or defeat $\sim vi$: to exert force in opposition syn see OPPOSE

resist n: something (as a protective coating) that resists or prevents a particular action
re-sis-tance \ri-zis-tan(t)\s\ n 1 a: an act or instance of resisting
: OPPOSITION b: a means of resisting 2: the ability to resist; esp : OPPOSITION b: a means of resisting 2: the ability to resist; esp: the inherent capacity of a living being to resist untoward circumstances (as disease, malnutrition, or toxic agents) 3: an opposing or retarding force 4 a: the opposition offered by a body or substance to the passage through it of a steady electric current b: a source of resistance 5 often cap: an underground organization of a conquered country engaging in sabotage and secret operations against occupation forces and collaborators

*re-sis-tant \(\gamma\)-tant\(\gamma\) adj: giving or capable of resistance — often used in combination (wrinkle-resistant clothes)

*re-sis-tant n: one that resists: RESISTER

used in combination (wrinkle-resistant clothes)

*resistant n: one that resists: RESISTER

re-sist-er \ri-'zis-tər\ n: one that resists; esp: one who actively
opposes the policies of a government

re-sist-ibil-i-ty \ri-zis-tə-'bil-ət-\ri\ n 1: the quality or state of
being resistible 2: ability to resist

re-sist-ible or re-sist-able \ri-'zis-tə-bəl\ adj: capable of being

resisted

re-sis-tive \ri-'zis-tiv\ adj: marked by resistance — ofte combination \(\)(fire-resistive material) — re-sis-tive-ly adv - often used in tive-ness n

re-sis-tiv-i-ty \ri-zis-'tiv-ət-ē, rē-\ n, pl-ties 1: capacity for re-sisting: RESISTANCE 2: the longitudinal electrical resistance of a uniform rod of unit length and unit cross-sectional area: the reciprocal of conductivity

re-sist-less \ri-'zist-less\adj 1: IRRESISTIBLE 2: offering no resistance — re-sist-less-ly adv — re-sist-less-ness n
re-sis-tor \ri-'zis-ter\n: a device that has electrical resistance and that is used in an electric circuit for protection, operation, or current control

• kitten a abut ər further a back ā bake ä cot. cart aŭ out ch chin e less ē easy i trip g gift ī life j joke ō flow o flaw òi coin th thin ŋ sing <u>th</u> this ü loot ù foot y yet vü few vù furious zh vision

EXHIBIT L-3

Ex. L-3 **LGD US PATENT No. 4,624,737**

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	PAGE
a process for producing a thin-film transistor	28
thin-film transistor	28
forming a gate electrode on an insulating substrate	7
forming on	7
continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film	9
continuously depositing	11
depositing on	11
depositing	11
gate insulating film	24
high-resistivity semiconductor film	34
conducting film	24
a conducting film containing at least a low-resistivity semiconductor film	24
low-resistivity semiconductor film	34
without exposing them to an oxidizing atmosphere	1
them	1
oxidizing atmosphere	1
selectively etched	40
they are partly left as an island region on said gate electrode	36
island region on said gate electrode	36
gate electrode	31

Ex. L-3 LGD US PATENT No. 4,624,737

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	AGE
a fourth step for selectively forming a source electrode and drain electrode	40
selectively forming	40
source electrode	31
drain electrode	31
contacting a part of the surface of said island region	36
a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask	18
selectively removing said conducting film exposed on said island region	18
selectively removing	21
said conducting film exposed on said island region	21
said source and drain electrodes serving as at least a part of the mask	13
serving as at least a part of the mask	13
at least a part of the mask	13
a part of the mask	13
mask	16
surface passivation film	43
exposing a part of each of said source electrode, drain electrode and gate electrode	43
exposing	43

EXHIBIT L-3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

without exposing them to an oxidizing atmosphere - without exposing the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the lowresistivity semiconductor film to an atmosphere that would create a detectable amount of oxidation on a film

them - the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film

oxidizing atmosphere - an atmosphere that would create a detectable amount of oxidation on a film

INTRINSIC EVIDENCE FOR DISPUTED TERM "WITHOUT **EXPOSING THEM TO AN OXIDIZING ATMOSPHERE":**

non would also occur at the interface of n+ amorphous silicon films 25, 26 and metal films 15, 16.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

1.45-59

phous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a

2.21-24

along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

As described above, according to the present invention, no oxides, etc., are formed at the interface of highresistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20, so that a good junction can be formed. The same is true with the interface of lowresistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity

3:53-59

<u>INTRINSIC EVIDENCE FOR DISPUTED TERM "WITHOUT</u> EXPOSING THEM TO AN OXIDIZING ATMOSPHERE" (cont'd):

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

4:3-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "THEM":

In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive depo-

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Page 8 of 48

INTRINSIC EVIDENCE FOR DISPUTED TERM "OXIDIZING **ATMOSPHERE**":

non would also occur at the interface of n+ amorphous silicon films 25, 26 and metal films 15, 16.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

1.45-59

phous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a

2.21-24

along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

As described above, according to the present invention, no oxides, etc., are formed at the interface of highresistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20, so that a good junction can be formed. The same is true with the interface of lowresistivity amorphous silicon film 20 and conducting film 30. Further, since the interfaces of low-resistivity

3:53-59

INTRINSIC EVIDENCE FOR DISPUTED TERM "OXIDIZING ATMOSPHERE" (cont'd):

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

4:3-12

EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

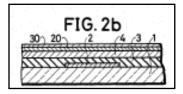
 A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode. drain electrode and gate electrode.

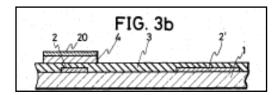
LGD's Claim Construction

forming a gate electrode on an insulating substrate - giving form or shape to a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode that is above and supported by or in contact with material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation

forming ... on - giving form or shape to...above and supported by or in contact with

INTRINSIC EVIDENCE FOR DISPUTED TERMS "FORMING A GATE ELECTRODE ON AN INSULATING SUBSTRATE" AND "FORMING... ON":





In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive depo-

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EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film - the formation of the gate insulating film, the highresistivity semiconductor film and conducting film (without intervening films) above and supported by or in contact with (i) the patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode and (ii) the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation

INTRINSIC EVIDENCE FOR DISPUTED TERM "CONTINUOUSLY DEPOSITING ON SAID GATE ELECTRODE AND SUBSTRATE A GATE INSULATING FILM, A HIGH-RESISTIVITY SEMICONDUCTOR FILM AND A CONDUCTING FILM":

[57] ABSTRACT

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

Abstract

In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive depo-

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EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

continuously depositing - the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films

depositing on - the formation of the gate insulating film, the highresistivity semiconductor film and conducting film above and supported by or in contact with

depositing - the formation of the gate insulating film, the highresistivity semiconductor film and conducting film

INTRINSIC EVIDENCE FOR DISPUTED TERMS "CONTINUOUSLY DEPOSITING," "CONTINUOUSLY DEPOSITING," AND "DEPOSITING ON":

In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film 3 from a mixed gas of SiH4 and NH3, forming a high-resistivity a-Si:H film 4 by using SiH4 and forming a n+ a-Si:H film 20 from a mixed gas of PH3 and SiH4 in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film 30 can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as

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along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

While the present invention has been principally described regarding an embodiment thereof as applied to the production of a thin-film transistor using amorphous silicon by utilizing plasma CVD, the invention can as well be applied to the manufacture of thin-film transistors using semiconductor films by utilizing the photo CVD or molecular beam and/or the ion beam deposition method, thin-film transistors using polysilicon, and thin-film transistors using semiconductor films of other

4:13-21

EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

 A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

said source and drain electrodes serving as at least a part of the mask - the source and drain electrodes serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed

serving as at least a part of the mask - serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed

at least a part of the mask at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed

a part of the mask - a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed

INTRINSIC EVIDENCE FOR DISPUTED TERMS "SAID SOURCE AND DRAIN ELECTRODES SERVING AS AT LEAST A PART OF THE MASK" AND "SERVING AS AT LEAST A PART OF THE MASK":

used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6. In this step, it is desirable to clean the surface of conducting film 30 by proper etching means such as sputter etching or ion

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INTRINSIC EVIDENCE FOR DISPUTED TERMS "AT LEAST A PART OF THE MASK" AND "A PART OF THE MASK":

used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6. In this step, it is desirable to clean the surface of conducting film 30 by proper etching means such as sputter etching or ion

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EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

mask - A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed

INTRINSIC EVIDENCE FOR DISPUTED TERM "MASK":

used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6. In this step, it is desirable to clean the surface of conducting film 30 by proper etching means such as sputter etching or ion

2:18-37

EXHIBIT 3 U.S. PATENT NO. 4,624,737 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask a fifth step for removing selected regions only of the conducting film on the island region not covered by the source electrode. drain electrode or mask wherein the source electrode and drain electrode serve as at least a part of the pattern above a surface from which material is to be selectively removed; the pattern is made of material that is resistive to the removal technique relative to the material to be removed

selectively removing said conducting film exposed on said island region - removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask

INTRINSIC EVIDENCE FOR DISPUTED TERM "FIFTH STEP FOR SELECTIVELY REMOVING SAID CONDUCTING FILM EXPOSING ON SAID ISLAND REGION WITH SAID SOURCE AND DRAIN ELECTRODES SERVING AS AT LEAST A PART OF THE MASK":

used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6. In this step, it is desirable to clean the surface of conducting film 30 by proper etching means such as sputter etching or ion

2:18-37

drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed. In this example, a chargeholding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resis- 3:38-50 tivity amorphous silicon film 20, but a conducting film

INTRINSIC EVIDENCE FOR DISPUTED TERM "SELECTIVELY REMOVING SAID CONDUCTING FILM EXPOSED ON SAID ISLAND **REGION":**

In the final step illustrated in FIG. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said

3:11-15

drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed. In this example, a chargeholding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resis- 3:38-50 tivity amorphous silicon film 20, but a conducting film

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

selectively removing removing selected regions only

said conducting film exposed on said island region - the conducting film on the island region that is not covered by the source electrode, drain electrode or mask

INTRINSIC EVIDENCE FOR DISPUTED TERM "SELECTIVELY **REMOVING":**

used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6. In this step, it is desirable to clean the surface of conducting film 30 by proper etching means such as sputter etching or ion

2.18-37

drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed. In this example, a chargeholding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resis- 3:38-50 tivity amorphous silicon film 20, but a conducting film

INTRINSIC EVIDENCE FOR DISPUTED TERM "SAID CONDUCTING FILM EXPOSED ON SAID ISLAND REGION":

In the final step illustrated in FIG. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said

3:11-15

drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed. In this example, a chargeholding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resis- 3:38-50 tivity amorphous silicon film 20, but a conducting film

ASSERTED CLAIM 1

 A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

gate insulating film - a thickness of non-conductive material (such as SiNx) that has a high electrical resistance and insulates the transistor gate from the semiconductor

conducting film - a thickness of electrically conductive material

a conducting film containing at least a low-resistivity semiconductor film - the conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films

<u>INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE INSULATING FILM":</u>

ing chamber is additionally provided, conducting film 30 can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film 3. In place of said high-resistivity amorphous silicon film 4, there can be used a film

2:34-39

INTRINSIC EVIDENCE FOR DISPUTED TERM "CONDUCTING FILM":

[57] ABSTRACT

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

Abstract

along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2.

3:47-52

INTRINSIC EVIDENCE FOR DISPUTED TERM "A CONDUCTING FILM CONTAINING AT LEAST A LOW-RESISTIVITY SEMICONDUCTOR FILM":

[57] ABSTRACT

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

Abstract

along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2.

3:47-52

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

a process for producing a thin-film transistor - a method for manufacturing thin-film transistors such as for a liquid crystal display

thin-film transistor - A threeterminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.

INTRINSIC EVIDENCE FOR DISPUTED TERM "A PROCESS FOR PRODUCING A THIN-FILM TRANSISTOR":

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. 1a to 1d illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. 1a in a sectional view is the initial step for selectively forming a gate electrode 2 on an insulating substrate 1 such as a glass substrate. Then, as shown in FIG. 1b, a gate insulating film 3 (such as silicon nitride film) and an amorphous silicon film 4 are continuously

3:6-19

1c. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. 1d, for instance n + amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit. If

3.26-33

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. 2a to 2e are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. 2a shows in a sectional view the initial step for selectively forming a gate electrode 2 on an insulating substrate 1 such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr. Mo, W. Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode 2.

4:6-17

INTRINSIC EVIDENCE FOR DISPUTED TERM "THIN-FILM **TRANSISTOR":**

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. 1a to 1d illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. 1a in a sectional view is the initial step for selectively forming a gate electrode 2 on an insulating substrate 1 such as a glass substrate. Then, as shown in FIG. 1b, a gate insulating film 3 (such as silicon nitride film) and an amorphous silicon film 4 are continuously

3:6-19

1c. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. 1d, for instance n + amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit. If

3.26-33

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. 2a to 2e are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. 2a shows in a sectional view the initial step for selectively forming a gate electrode 2 on an insulating substrate 1 such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr. Mo, W. Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode 2.

4:6-17

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

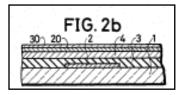
LGD's Claim Construction

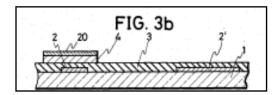
gate electrode - a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode

source electrode - a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode

drain electrode - a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode

INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE ELECTRODE":





In the next step illustrated in FIG. 2b in a sectional view, a gate insulating film 3, a high-resistivity film 4, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film 20 and a conducting film 30 made of a metal or other material are successively formed on said gate electrode 2 and substrate 1 without exposing them to an oxidizing atmosphere. Such successive depo-

2:18-24

INTRINSIC EVIDENCE FOR DISPUTED TERMS "SOURCE ELECTRODE" AND "DRAIN ELECTRODE":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-62

In the next step illustrated in FIG. 3c, a transparent conducting film such as ITO film is deposited; then, drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous

3:36-40

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

high-resistivity semiconductor **film** - a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous siliconfluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the lowresistivity semiconductor film

low-resistivity semiconductor

film - a thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous siliconfluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon which contains phosphorous or other impurities to enhance the conductivity of the film) that has a lower resistance to current flow relative to the highresistivity semiconductor film

INTRINSIC EVIDENCE FOR DISPUTED TERMS "HIGH-RESISTIVITY SEMICONDUCTOR FILM" AND "LOW-RESISTIVITY FILM":

to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film 3. In place of said high-resistivity amorphous silicon film 4, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF4, or a microcrystalline amorphous silicon film. Such alloys can be also used for said low-resistivity amorphous silicon film 20, and such film may contain other impurites beside phosphorous impurities.

2:34-45

along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate. Then, as illustrated in FIG. 3b, gate insulating film 3, high-resistivity amorphous silicon film 4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are

3:26-33

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

they are partly left as an island region on said gate **electrode** - a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor

island region on said gate **electrode** - a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor

contacting a part of the surface of said island **region** - touching a part of the surface of the island region

INTRINSIC EVIDENCE FOR DISPUTED TERM "THEY ARE PARTLY LEFT AS AN ISLAND REGION ON SAID GATE ELECTRODE":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-61

4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed.

INTRINSIC EVIDENCE FOR DISPUTED TERM "ISLAND REGION ON SAID GATE ELECTRODE":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-61

4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed.

INTRINSIC EVIDENCE FOR DISPUTED TERM "CONTACTING A PART OF THE SURFACE OF SAID ISLAND REGION":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-61

4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed.

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

LGD's Claim Construction

selectively etched - The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface

a fourth step for selectively forming a source electrode and drain electrode - forming a source electrode and drain electrode in selected regions only

selectively forming - forming in selected regions only

INTRINSIC EVIDENCE FOR DISPUTED TERMS "SELECTIVELY ETCHED" AND "A FOURTH STEP FOR SELECTIVELY FORMING A SOURCE ELECTRODE AND DRAIN ELECTRODE":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-61

4 and low-resistivity amorphous silicon film 20 are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed.

INTRINSIC EVIDENCE FOR DISPUTED TERM "SELECTIVELY FORMING":

FIG. 2c illustrates the step in which said conducting film 30, low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15,

2:54-62

In the next step illustrated in FIG. 3c, a transparent conducting film such as ITO film is deposited; then, drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous

3:36-40

EXHIBIT 3 U.S. PATENT NO. ____ TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

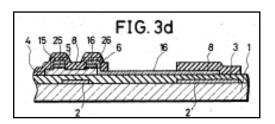
LGD's Claim Construction

surface passivation film - a thickness of material that provides protection such as electrical stability and chemical isolation

exposing a part of each of said source electrode, drain electrode and gate electrode removing portions of one or more layers to uncover a part of each of said source electrode, drain electrode and gate electrode

exposing - removing portions of one or more layers to uncover

INTRINSIC EVIDENCE FOR DISPUTED TERM "SURFACE **PASSIVATION FILM":**



5, 6, thereby completing a thin-film transistor unit. If necessary, a surface passivation film and/or light-shielding film are further formed thereon.

In the conventional process shown in FIGS. 1a to 1d, since the masking step precedes the deposition of n+

2:54-62

In the final step illustrated in FIG. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said surface passivation film 8. If light shielding is required, a multilayer film composed of said insulating film and a metal or high-resistivity semiconductor film can be used as said surface passivation film 8. When amorphous silicon-germanium alloy (a-Si_{1-x}Ge_x) is used as lightshielding film, surface passivation may not be necessary.

holding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode

3:42-47

INTRINSIC EVIDENCE FOR DISPUTED TERMS "EXPOSING A PART OF EACH SAID SOURCE ELECTRODE, DRAIN ELECTRODE AND GATE ELECTRODE" AND "EXPOSING":

In the final step illustrated in FIG. 2e, a surface passivation film 8 is deposited, and the drain and source electrodes 15, 16 and gate electrode 2 are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a 2:54-62 resist or a coating of polyimide resin can be used as said

drain electrode 15 and source electrode 16 which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film 20 is removed. In this example, a chargeholding capacitor is formed by said picture cell electrode (source electrode) 16, gate electrode 2' and gate insulating film 3. In the final step shown sectionally in FIG. 3d, surface passivation film 8 concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode 15 and a part of gate electrodes 2, 2' (not shown). In this example, no conducting film is formed on low-resis- 3:38-50 tivity amorphous silicon film 20, but a conducting film

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LGE as a party. On October 12, 2004, this Court denied LPL's motion to stay NED NED further proceedings pertaining to the side-mount patents and set the claim construction hearing for January 7, 2005. On its own motion, the Court continued the claim construction hearing to January 13, 2005.

LEGAL STANDARD

In interpreting an asserted claim, the Court first looks to the intrinsic evidence, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576 (Fed. Cir. 1996). However, all intrinsic evidence is not equal. First, the Court should focus on the claims themselves, both asserted and unasserted, to define the meaning and scope of the patented invention. Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193, 1201-02 (Fed. Cir. 2002). There is a "heavy presumption" that the ordinary and accustomed meaning of a claim term, as understood by one of ordinary skill in the art, is the correct construction. CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d 1359, 1366 (Fed. Cir. 2002). Dictionaries, encyclopedias and treatises, which are extrinsic evidence, may be employed to "assist the court in determining the ordinary and customary meanings of claim terms." Texas Digital, 308 F.3d at 1202.

Second, the Court should review the specification. Vitronics, 90 F.3d at 1582. A review of the specification will reveal whether or not the inventor has given a term an unconventional meaning. *Id.* However, it is improper to read a limitation into a claim from the specification. Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182 (Fed. Cir. 1998). The inventor may act as his or her own lexicographer and use terms in a manner other than their ordinary meaning, so long as any such specific definition is clearly stated in the patent specification or prosecution history. Mycogen Plant Science Inc. v. Monsanto Co., 243 F.3d 1316, 1327 (Fed. Cir. 2001). Therefore, for claim construction purposes, the specification is "the single best guide to the meaning of a disputed term."

Vitronics, 90 F.3d at 1582.

Third, the Court may consider the prosecution history of the patent. The prosecution history is significant because it reveals "the course of dealing with the Patent Office, which may show a particular meaning attached to the terms, or a position taken by an applicant" to secure the patent. *Markman*, 52 F.3d at 991. As such, the prosecution history may be reviewed to assess whether a patentee "relinquished [a] potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a [prior art] reference." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999), *cert. denied*, 529 U.S. 1066 (2000). However, for subject matter to be held relinquished, a court must find that the patentee disclaimed the subject matter with "reasonable clarity and deliberateness." *Northern Telecom Ltd. v. Samsung Electronics Co., Ltd.*, 215 F.3d 1281, 1294 (Fed. Cir. 2000).

Finally, if and only if a claim remains "genuinely ambiguous" despite the full consideration of the intrinsic evidence, then a court may look toward extrinsic evidence to interpret the claim term itself. *Bell & Howard Document Mgmt*.

Prods. Co. v. Altek Sys., 132 F.3d 701, 706 (Fed. Cir. 1997). The need for such a departure from the intrinsic evidence "rarely, if ever, occurs." Vitronics, 90 F.3d at 1585.

ANALYSIS

A. Side-Mounting Patents

The side-mounting patents consist of U.S. Patents Nos. 6,373,537 ('537 patent), 6,00,457 ('457 patent), 6,020,942 ('942 patent), and 5,926,237 ('237 patent).

1. Whether the Side-Mounting Patents Are Limited to Portable Computers

The definition of the terms "liquid crystal display," "liquid crystal panel," "housing" and "outer casing" are disputed because CPT limits them to "portable

computers" whereas LPL does not so limit them. The '537 and '237 patents whereas the '457 patent contains claims directed only to the LCD device and the '942 patent contains claims. '942 patent contains claims directed only to a portable computer. Since the Court 4 must look first to the claims, the Court finds that claims that recite a "portable computer" are limited to portable computers, but claims that do not recite a "portable computer" are not so limited. The background of the invention also indicates that the portable computer is an example of a device that uses an LCD. See, e.g., 1:50-51 ("[t]he liquid crystal display is usually combined with, for example, a notebook computer for use as an output screen"; 1:59-61 ("a liquid crystal display is attached to a device such as a notebook computer"). With respect to the terms "housing" and "outer casing," the Court notes that independent claims, such as Claim 37 of the '457 patent, which contain the term "housing" do not contain the words "portable computer," whereas dependent claim 40 of the '457 patent states "the housing includes a portable computer." This indicates that the definition of the terms should not be limited to a portable computer.

Defendants look at the specification, rather than first looking to claims, in arguing that the invention described in the specification is directed to an improvement for a portable computer. Defendants' argument is not persuasive, as the Federal Circuit has held that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction." Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004); accord Gemstar-TV Guide Int'l Inc. v. ITC, 383 F.3d 1352, 1366 (Fed. Cir. 2004). The specification of the sidemounting patents does not contain any "clear disavowal" of products that are not portable computers. In addition, this Court rejects Defendant's argument that the

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sidemounting patents should be limited to portable computers because that was the purported "object" of the invention. "The fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives." Liebel, 358 F.3d at 908. See also Ex-Pass Tech, Inc. v. 3Com Corp., 343 F.3d 1364, 1370 (Fed. Cir. 2003) ("The Court's task is not to limit claim language to exclude particular devices because they do not serve a perceived "purpose" of the invention."). Thus, the Court adopts LPL's definitions of the terms "liquid crystal display," "liquid crystal panel", "housing" and "outer casing."

2. Whether Constructions Should Include the Word "Directly"

The word "directly" does not appear anywhere in the claim language. However, Defendants use the word "directly" in construing the terms "attachable to a housing," "fixable to a housing," "joined with," "joining together," "coupled," and "fastening part." Defendants argue that the claim language, in context, indicates that side-to-side direct connection must be present, as the specification does not show any intervening element. The Court finds Defendants' arguments unpersuasive pursuant to *Liebel*, which makes it clear that the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction. Since no such words of manifest exclusion or restriction are used here, the Court adopts LPL's definitions of "attachable to a housing" or "fixable to a housing," "joined," "joined together," "coupled," and "fastening part."

Whether the terms "through" and "passing through" should have 3. different meanings

LPL proposes that the term "through" be used in its plain and ordinary way to mean "by way of," and that "passing through" means "extending into." Defendants contend that "through" means "in at one end, side or surface and out

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the other" and that "passing through" means "moving past or making way in one side and out of the other side." Although the preferred embodiment shown in the drawings uses screws engaging holes to connect the components, the patent clearly contemplates other methods of attaching the components. The '457 patent specification, for example, provides that "an adhesive device, such as double-sided tape can be used instead of the second and third screw holes" and that "the rear case 500 and the second support frame 400 are jointed to each other using hooks and/or other suitable fastening devises, including adhesives." See, e.g., 4:58-60, 4:63-67. Since LPL's definition of "through" covers both screws and adhesives, the Court finds that it is the better definition.

LPL contends that the phrase "passing through," in contrast to "through," is used only in reference to screws and screw holes, which extend into an object. CPT, on the other hand, argues that "passing through" and "through" have the same meaning. The doctrine of claim differentiation indicates that different words or phrases used in different claims are presumed to indicate that the claims have different meaning and scope. Karlin Tech, Inc. v. Surgical Dynamics, Inc., 177 F.3d 968, 971 (Fed. Cir. 1999). Here, it appears that the inventors used the term "through" when generally referring to a fastening part but used "passing through" only when referring to a specific fastening part (i.e., a screw). Therefore, the Court adopts LPL's definitions of "through" and "passing through."

Whether the terms "frame," "first frame," and "second frame" 4. should be given their plain and ordinary meanings.

LPL defines "frame" to mean "a support structure." Defendants defines "Frame" as "an open structure or rim for encasing, holding or bordering that encloses a substantial portion of each side edge of another structure." Defendants base their argument on the theory that the meaning of the word "frame" is limited to the description in the specification. Under Liebel, this restrictive interpretation is inappropriate. Furthermore, Defendants define "first" and "second" frame to

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mean "inner" and "outer" frame, even though the inventors did not use those terms. The use of "first" and "second" follow the "common patent-law convention to distinguish between repeated instances of element or limitation." 3M Innovative Properties Co. v. Avery Dennison Corp., 350 F.3d 1365, 1371 (Fed. Cir. 2003). For example, Claim 31 of the '942 patent claims "[t]he portable computer according to claim 13 wherein the fastening part includes first and second screws passing through first and second holes at a same side edge of at lease one of the first and second frames." 8:25-28. Here, the words "first" and "second" are consistently used to distinguish repeated instances of element or limitation. Therefore, the Court gives "frame," "first frame" and "second frame" their ordinary meanings, as set forth by LPL.

5. Whether "liquid crystal display model" is a typographical error

The parties agree on the construction of the claim term "liquid crystal display module." However in one claim, Claim 7 of the '537 patent, the term appears as "liquid crystal display model." Given the context, this is clearly a typographical error. Other parts of Claim 7 refer to the "liquid crystal display module." The Court therefore construes "liquid crystal display model" as "liquid crsytal display module."

6. Whether Definitions are Needed for "Portable Computer," "Side", "Forming" and "Cover"

Defendants propose cumbersome definitions for the terms "portable computer," "side", "forming" and "cover." The Court finds that these definitions create unnecessary confusion and adopts LPL's constructions, which give the terms their plain and ordinary meaning.

B. Construction of the '737 Semiconductor Patent

1. "Source Electrode," "Drain Electrode," and "Gate Electrode"

While LPL construes the electrode to include the line and the pad, Defendants limits the electrode to a single TFT and construes the electrodes as

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distinct from the lines and the pads. The seventh step of claim 1 of the '737 patent calls for "exposing a part of each of said source electrode, drain electrode and gate electrode." LPL persuasively argues that electrodes are exposed at the pad region for electrical connection, as exposing a gate pad allows electrical control of all TFT gate contacts along the row. One of ordinarily skill would not control each TFT gate/source independently, especially since creating a hole at each TFT to expose the gate electrode would destroy the TFT. Furthermore, the specification of the '737 patent describes a step in which "gate electrode 2 extending along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate." 3:25-28. This indicates that a structure separate from the TFT is part of the "gate electrode." In addition, the claims in the application for the '449 patent include phrases such as "said pad comprising: a portion of said data electrode" and "a pad including a portion of [said] data electrode." Finally, U.S. Patent 4,705,358 ('358 patent), which also pertains to the same technology as the '737 patent, names the same inventor as the '737 patent, and was filed in the U.S. on the same day as the '737 patent, illustrates a gate electrode from above (i.e. a "bird's-eye-view") and demonstrates that the "gate electrode" may include the gate line. The Court therefore finds that the electrodes may include the lines and pads. Furthermore, the Court is not persuaded by that portion of Defendant's construction which specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Continuously Depositing"

LPL construes the term "continuously depositing" as "[t]he formation of the gate insulting film, the high-resistivity semiconductor film and conducting film without intervening films." Defendants offer a modified construction of this term

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as meaning that "the deposition of the specified films occurs without any nondeposition related steps between or during the deposition of each constituted film." While LPL's definition requires the films to be only spatially continuous. Defendants' definition requires continuity in space, time and sequence. The '737 patent shows "continuously deposited" films as being spatially continuous, but it does not show, mention or require the deposition to be performed without an interruption in time or sequence. Moreover, the plain meaning of "continuous" is "uninterrupted extension in space, time or sequence." The Court therefore adopts LPL's construction of "continuously depositing."

3. "Oxidizing atmosphere"

Claim 1 of the '737 patent requires "continuously depositing [the films]... without exposing them to an oxidizing atmosphere." LPL construes "an oxidizing atmosphere" as "an atmosphere that would create substantial oxidation on a film." The Court finds that the word "substantial" in this construction is vague and ambiguous. Defendants initially construed this phrase to mean that the films are not permitted to be exposed to "an oxide," although they acknowledged that a de minimus amount of oxidation is not an "oxidation atmosphere." Defendants subsequently modified their construction to be "an atmosphere that would create a detectable amount of oxidation on a film." As "detectable" is more precise than "substantial," the Court adopts Defendants' modified construction of this term.

4. "Island region"/ "island region on said gate electrode"

At the time the patent application was filed, there were at least two wellknown constructs for the semiconductor region in a TFT. In one design, separate islands of semiconductor are created above each TFT's gate electrode. In the other design, a single, unitary semiconductor region extends over all of the TFTs in one large "continent." While LPL construes the term "island region" as used in the '737 patent to include both designs, Defendants' construction limits this term to the first design (i.e. a region located over the gate electrode of a single TFT).

Defendants also require the island to have been "etched around its entire perimeter."

Defendants' argument is persuasive, as claim 1 recites a process for producing "a thin-film transistor." 4:26. See also 1:5, 13, 29, 57, 65, 67; 2:9; 3:34-35. Furthermore, in discussing FIG. 3b, the specification provides that "said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed." 3:34-35. This statement indicates that the "island region" is limited to the area of a single TFT and does not include multiple TFTs. Thus, the Court finds that Defendants' construction more accurately reflects the language of the claim and the specification. Moreover, LPL's construction appears to read the term "island region" completely out of the third step, "in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode." The Court therefore adopts Defendants' construction of the term "island region."

5. "Conducting Film Containing at Least a low-resistivity
Semiconductor Film"/ "Conducting Film"/ "High-resistivity
Semiconductor Film"/ "Low-Resistivity Semiconductor Film"

The '737 patent discloses two preferred embodiments. One embodiment includes four continuously deposited films: an insulating film, a high-resistivity semiconductor films, a low-resistivity semiconductor film, and a conducting film. *See* 2:17-21, Fig. 2a-2e. The other embodiment has three continuously deposited films: an insulating film, a high-resistivity semiconductor films, and a low-resistivity semiconductor film. *See* 2:24-30, Fig. 3a-3d.

Claim 1 of the '737 patent sets forth "a second step for continuously depositing . . . a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low -resistivity semiconductor film." Claim 2, which is not at issue in this litigation, sets forth a second step wherein "said

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conducting film is composed of at least two layers consisting of a low-resistivity semiconductor films and thereon a refractory metal film or transparent conducting film."

According to LPL, the italicized phrase in Claim 1 above means that the conducting film may consist only of a low-resistivity semiconductor film. CPT, on the other hand, construes this phrase as requiring a conducting film with adjoining layer of low resistivity semiconductor and possibly other adjoining layers. CPT relies on a sentence in the specification discussing Fig. 3a-3d, which states that, "[i]n this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2." While this sentence does suggest that the conducting film is distinct from the low-resistivity semiconductor film, CPT's interpretation would narrow the scope of Claim 1 to exclude the second embodiment. A claim construction that excludes a preferred embodiment is "rarely, if ever, correct." Dow Chemical Co. v. Sumitomo Chemical Co., 257 F.3d 1364, 1378 (Fed. Cir. 2001). Furthermore, the fact that the conducting film is specifically described as having two layers in claim 2 but not in claim 1 indicates that two adjoining layers are not needed for the first claim. Thus, the Court adopts LPL's construction of the term "conducting film containing at least a low-resistivity semiconductor film."

LPL's construction of "conducting film" is consistent with this Court's determination that the conducting film can be the low -resistivity semiconductor film. LPL construes "conducting film" according to its plain meaning, namely, a thickness of electrically conductive material. Defendants' construction of conducting film, on the other hand, restricts it to film "having an electrical

¹LPL submits intrinsic evidence in the form of a scientific article describing ITO (indium tin oxide) as a "semiconductor." This supports LPL's position that the conducting film can be the low-resistivity semiconductor.

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resistance several order of magnitude lower than a low-resistivity semiconductor film." In other words, Defendants define "conducting film" as distinct from "lowresistivity semiconductor film." The Court rejects Defendants' construction and adopts LPL's construction since it finds that the conducting film in claim 1 of the '737 patent may consist of the low-resistivity semiconductor film, as discussed above.

LPL's constructions of "high-resistivity semiconductor film" and "lowresistivity semiconductor film" distinguishes these terms based on their relative resistivity. Defendants distinguish the terms according to whether they are "doped" (i.e. intentionally mixed with impurities) or "undoped." The '737 patent makes no mention of the terms "doped" and "undoped." Furthermore, LPL presents evidence that it is improper to equate the terms high-resistivity with "undoped" and low-resistivity with "doped." The Court therefore rejects Defendants' method of distinguishing these terms. Defendants also rely solely on extrinsic evidence in defining high-resistivity semiconductor film as having a resistence "many orders of magnitude" greater than the low-resistivity film. The Court finds this language vague and unnecessary. The Court therefore adopts LPL's constructions of the terms "high-resistivity semiconductor film" and "lowresistivity semiconductor film."

"Mask"/ "At least a part of the Mask"/ "Said source and drain electrodes serving as at least part of the mask"

Claim 1 requires a step for selectively removing material "with said source and drain electrodes serving as at least part of the mask." The parties dispute whether an electrode covered by photoresist serves as at least part of the mask. Defendants' construction may exclude such an electrode, as it requires that the source and drain electrodes "make a *significant contribution* to defining the edges of the selectively removed region" or alternatively "shield at least part of the surface from the action of the removal technique." While the photoresist may be

the *outermost* layer of the mask, the electrodes are part of the mask structure, as, they, too, are resistive to the removal technique and in the pattern needed to etch exposed conductive film. LPL construes "mask" as "a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed." The Court finds that this definition best explains the mask, as well as how the electrodes serve as "at least a part of the mask." The Court does not need to construe "said source and drain electrodes serving as at least part of the mask," since this phrase simply combines the terms "source electrode," "drain electrode" and "at least a part of the mask."

7. "Thin Film Transistor"

LPL's and Defendants' construction of "thin film transistor" ("TFT") are very similar. They differ in one respect: LPL specifies that TFTs are not constructed in a single crystal silicon wafer. Since the single wafer is mentioned in the intrinsic evidence and Defendants do not deny that TFTs are constructed in a single crystal silicon wafer, the Court adopts LPL's construction.

8. "A fourth step for selectively forming a source electrode and drain electrode"

LPL's construction of "a fourth step for selectively forming a source electrode and drain electrode" requires the source and drain electrodes to be "formed together." The Court finds nothing in the claim or specification that supports this interpretation. Although the formation of the source and drain electrodes is listed in one step, nothing suggests that each action within each step must be performed together. LPL's argument that the objective of the invention supports this interpretation is unpersuasive in light of *Liebel*, discussed above. However, the Court also finds Defendants' construction problematic. Defendants construe this phrase as "forming a source electrode and drain electrode in selected regions only by depositing a conducting film or other material such as Al."

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Figures 1-3 and the specification do indicate that the source and drain electrode are formed in selected regions. See 1:15-17, 2:10-14,, 3:36-44. However, the specification does not support the second part of CPT's construction. Rather, the specification indicates that source and drain electrodes can be formed via deposition and subsequent etching of conductive material. The Court therefore modifies Defendant's construction and defines the phrase as "forming a source electrode and drain electrode in selected regions only," which is consistent with the Court's construction of "selectively forming" below.

"Contacting a part of the surface of said island region" 9.

LPL construes "contacting a part of the surface of said island region" to mean "[f]orming an electrical connection to a part of the surface of the island region" while Defendants construe it to require "touching a part of the surface of the island region." The Court finds that Defendants' construction better reflects the plain meaning of the claim.

"Forming ... on" 10.

The first step of claim 1 is "for forming a gate electrode on an insulating substrate." LPL argues that the '737 patent uses "forming" in the sense of "providing" whereas Defendants construe "forming" as to give "form or shape to." The Court finds it awkward to define "forming" as "providing" in the phrase "selectively forming a gate electrode 2 on an insulating substrate 1," which is offered as intrinsic evidence by both parties. Defendants' construction is more meaningful in this specific context as well as in the specification and the claims as a whole. Moreover, Defendant's construction is consistent with this Court' definition of "a fourth step for selectively forming a source electrode and drain electrode." The Court therefore adopts Defendants' construction of "forming... .on."

"Selectively etched"/ "Selectively forming"/ "Selectively 11. removing"

Claim 1 recited a third step wherein "said high-resistivity semiconductor film and said conducting films are selectively etched so that they are partly left is an island region on said gate electrode." LPL defines "selectively etched" as the "removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface." Defendants object to this definition because it refers to removal of portions of a surface, rather than the entire film. While the claim does specifically refer to the etching of the high-resistivity semiconductor film and the conducting films, the Court finds nothing in the language of the claim or the specification that requires etching of the entire film. Furthermore, Defendants' construction, which requires etching of the high-resistivity semiconductor film, the conducting film, and the low-resistivity semiconductor film, is inconsistent with both the language of the claim and with this Court's finding that the conducting film may constitute the low-resistivity semiconductor film. The Court therefore adopts LPL's definition of "selectively etched."

In addition, Claim 1 recites a fourth step for "selectively forming a source electrode and a drain electrode," and a fifth step for "selectively removing said conducting film exposed on said island region." The Court finds no substantive difference between LPL's and Defendants' constructions of "selectively forming" and "selectively removing." However, the Court adopts Defendants' definitions of these respective terms as "forming in selected regions only" and "removing selected regions only" because they convey the meaning in the simplest language.

C. Construction of Disputed Terms of the '449 Patent

1. Gate Electrode/ Source Electrode

Defendants construe the gate/ source/ data electrodes to exclude the lines and pads. Claims 10 and 11 of the '449 patent do refer to the gate electrode, gate pad, source electrode, and source pad individually. For example, claim 10 recites that the liquid crystal display device is comprised of "a first conductive layer...

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including: a gate electrode, a gate pad, and a source pad." (7:34-39). The specification, however, provides additional information that helps clarify the relationship between the electrodes and the pads. In Figures 2d and 2e, the source pad and source electrode are shown as one connected structure, although they are labeled 7 and 7A respectively. In discussing Figure 2c, the specification states that "source electrode 7 thus forms part of a transistor region and serves as source pad 7A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT." (4:1-5). In discussing Figure 2e, the specification states that "ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD." In describing the second embodiment depicted in Figure 3, the specification provides that "source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed." Thus, while the source pads and electrodes are formed separately, they are then connected and the specification's language indicates that they are not necessarily distinct structures. The originally filed application during the prosecution of the '449 patent also supports LPL's position that the electrode should not be defined as excluding the line and pad. The first claim of the original application recites "[a] pad for providing an[] electrical connection to a data electrode of a switching device, said pad comprising: a portion fo said data electrode " The fourth claim in the original application recites "a liquid crystal display device comprising: a data line; and a pad, said pad including: a portion of said data line. . . . " Likewise, the intrinsic evidence does not indicate that the gate electrode must exclude the gate pad. In fact, Figures 2a-2e do not include a separate number identifying the "gate electrode." The Court therefore rejects a construction of "electrode" that specifically excludes the line and pad.

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²The word "data" corresponds to "source."

The Court also rejects Defendant's construction of these terms because it specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The intrinsic evidence does not support such a limitation. Furthermore, as discussed previously with respect to the '737 patent,' the embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Gate pad"/ "Source pad"

According to LPL's construction, pads are provided near the periphery of the TFT array "to receive data from a [gate or data] driving circuit." Defendants contend that this is ambiguous because other parts of the wiring, which are not pads, may also receive data from an external driving circuit. Defendants construe the pads as an element "that is necessary in order to communicate information from an external driving circuit to a [gate or source] electrode." Defendants base this construction on a sentence in the specification which states that "a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source." (1:51-53). Since the specification refers to the pad wiring layer as being necessary and not the pad, the Court rejects Defendants' construction and adopts LPL's constructions of "gate pad" and "source pad."

3. "On"/ "formed on"/ "disposed on"

LPL defines "on", "formed on" and "disposed on" as "touching a top or side of." LPL contrasts these terms with "overlying," which it defines as "above" something but not necessarily touching it. This Court agrees with Defendants that the specification does not support the distinction made by LPL. For example, the specification states that a "conductive layer is formed *on* the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8." (5:6-8) (emphasis added). Conductive layer 7 and 8 do not touch the substrate (see Fig. 3), yet the specification uses the word "on." *See*

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also 2:42-44; 3:50-54; 7:49-50 (all using the word "on" to describe a situation where there is no "touching"). The Court therefore adopts Defendants' definition of "on."

4. "Contact hole is provided through . . . layer"/ "Provided through"

The phrases "contact hole is provided through" and "provided through" appear only in claims 1 and 10, always in the context of a contact hole being "provided through" one or more layers of materials. Defendants construe the claim terms to mean that these holes are "made in one side and out the opposite side" of the layers of materials. The Court finds that these phrases should be given their ordinary meaning and therefore adopts LPL's constructions.

5. "Active layer"

Defendants' construction of "active layer" limits this area to the region of the semiconductor layer that forms the channel region between the source and drain electrodes. Figures 2b-e, 3 and 5 of the specification show the active layer 4 extending only under the source 7 and drain 8. However, as LPL points out, these figures do not in any way limit the extension of active layer 4 in the dimension perpendicular to the figure, or in other areas of the substrate not depicted in the cross-section views. Since nothing in the claim or specification limits the active layer to the region of semiconductor layer between the source and drain electrodes, the Court adopts LPL's construction of this term.

6. "Common hole"

LPL construes "common hole" in accordance with its plain meaning as "[a] shared hole." Defendants construe "common hole" to mean "single hole." The court finds Defendants' construction ambiguous, since it suggests that only one hole is permitted. The Court therefore adopts LPL's construction of this term.

7. "Aligned"

LPL construed "aligned" to mean "placed in line with," which is its ordinary meaning. Defendants, on the other hand, construe "aligned" to mean

"substantially co-axial or concentric." Defendants' definition would require the holes to be one on top of the other, whereas LPL's construction would permit the holes to be placed either side-by-side or on top of each other. Although the figures in the specification show these holes to be on top of each other as described by Defendants, the plain language of the claim should not be limited by the figures in the specification. *See Dayco Products*, 258 F.3d at 1327. The Court therefore adopts LPL's construction fo this term.

8. "Said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region"

Defendants' construction of "said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region" limits the phrase to mean that "the first and second contact holes must overlap." However, none of the embodiments disclosed in the '449 patent teaches that the hole exposing the second conductive layer (i.e. the "second hold") overlaps with the hole in the first insulative layer that exposes the first conductive layer. *See, e.g.,* Fig. 3 and Fig. 5. Since a claim construction that excludes from its scope a preferred embodiment is rarely, if ever, correct, the Court adopts LPL's construction.

9. "Wiring structure"

This term "wiring structure" appears in Claims 1-5 of the '449 patent. LPL's definition characterizes the term as a "slender structure" while Defendants refer to the layer simply as a "structure." Claim 1 begins with "A wiring structure comprising: a substrate" Since the substrate is typically a large slab of glass, which is not "slender," the Court adopts Defendants' definition of this term.

IT IS SO ORDERED

DATE: May 5, 2005

CONSUELO B. MARSHALL UNITED STATES DISTRICT JUDGE

EXHIBIT L-4(b)

Document 389-9

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Case 1:06-cv-00726-JJF

1 LG.PHILIPS LCD CO., LTD., 2 Plaintiff, 3 VS. 4 LITE-ON TECHNOLOGY CORP. and LITE-ON TECHNOLOGY 5 INTERNATIONAL INC., 6 Defendants. 7 LG.PHILIPS LCD CO., LTD., 8 Plaintiff, 9 VS. 10 TPV TECHNOLOGY, LTD, and ENVISION PERIPHERALS, INC., 11 12 Defendants. 13 LG.PHILIPS LCD CO., LTD., 14 Plaintiff, 15 VS. 16 VIEWSONIC CORPORATION, 17 Defendant. 18

Pursuant to the Court's October 1, 2003 Order regarding Claim Construction Briefing, LG.Philips LCD Co., Ltd. ("LPL"), Tatung Co. of America and Tatung Company (collectively "Tatung"), Chunghwa Picture Tubes, Ltd. ("CPT"), Jean Company, Ltd. ("Jean Co."), Lite-On Technology Corporation and Lite-On Technology International Incorporated (collectively "Lite-On"), TPV Technology, Ltd. ("TPV"), Envision Peripherals, Inc. ("Envision") and Viewsonic Corporation ("Viewsonic") submit this Second Revised Joint Claim Construction Statement consisting of Exhibits A-F.

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Exhibit A is a list of claim terms for which the parties agree on a construction concerning U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237. Exhibit A is submitted on behalf of all of the parties.

Exhibit B is a list of disputed terms from U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237, along with the parties' respective constructions and support for those constructions. Exhibit B is submitted on behalf of all of the parties.

Exhibit C is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 4,624,737. Exhibit C is submitted on behalf of all of the parties.

Exhibit D is a list of disputed terms from U.S. Patent No. 4,624,737, along with the parties' respective constructions and support for those constructions. Exhibit D is submitted on behalf of all of the parties.

Exhibit E is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 5,825,449. Exhibit E is submitted on behalf of all of the parties.

Exhibit F is a list of disputed terms from U.S. Patent No. 5,825,449, along with the parties' respective constructions and support for those constructions. Exhibit F is submitted on behalf of all of the parties.

Exhibits A-F filed herewith will supercede Exhibits A-F of the Revised Joint Claim Construction Statement, filed on September 17, 2003 ("First Revised JCC"). In addition, all supporting exhibits filed by the parties in support of their respective positions are incorporated herein.

Defendants' submission of these proposed claim constructions and corresponding support should not be construed as an admission by any defendant that any of the claims are infringed, valid or enforceable. Defendants' submissions relate to those patents asserted against them in the various Complaints.

Furthermore, defendants' submission of these proposed claim constructions do not 1-LA750383.1

affect or waive any arguments regarding the invalidity of the patents-in-suit. The parties preserve the right to amend and/or supplement the terms and/or constructions in the attached claim charts as claim construction discovery continues and as the parties continue

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Page 6 of 108

1	to meet and confer to reduce the n	umber of claims asserted and to reduce the
2	number of terms for the Court to c	construe.
3	Dated: December, 2003	JEFFREY N. BROWN TERESA A. MACDONALD
5		ANN A. BYUN ANTHONY C. ROTH NATHAN W. McCUTCHEON
6		MORGAN, LEWIS & BOCKIUS LLP
7	·	By
8		Jeffrey N. Brown Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
9	Dated: December 23, 2003	MARK KRIETZMAN
10	_	CHRISTOPHER DARROW VALERIE W. HO
11 12	•	GREENBERG TRAURIG LLP
13		By
14		Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December, 2003	TERESA M. CORBIN
16		GLENN W. RHODES CHRISTOPHER A. MATHEWS BRIAN S. Y. KIM
17		HOWREY SIMON ARNOLD & WHITE LLP
18		Ву
19		Christopher A. Mathews Attorneys for Defendants/Counterclaimants CHUNGHWA PICTURE TUBES, LTD., JEAN
20		CHUNGHWA PICTURE TUBES, LTD., JEAN COMPANY, LTD., LITE-ON TECHNOLOGY
21	·	COMPANY, LTD., LITE-ON TECHNOLOGY CORPORATION, LITE-ON TECHNOLOGY INTERNATIONAL INCORPORATED, TPV TECHNOLOGY LTD. and ENVISION PERIPHERALS, INC.
22		TECHNOLOGY LTD. and ENVISION PERIPHERALS, INC.
23	Dated: December, 2003	SCOTT R. MILLER TRACY R. ROMAN
25		TRACY R. ROMAN BINGHAM McCUTCHEN LLP
26		By
27		Scott R. Miller
28		Attorneys for Defendant VIEWSONIC CORPORATION
	1PW/1933229 1	

1	to meet and confer to reduce the nu	umber of claims asserted and to reduce the
2	number of terms for the Court to c	onstrue.
3	Dated: December, 2003	JEFFREY N. BROWN TERESA A. MACDONALD
4		ANN A. BYUN
5		ANTHONY C. ROTH NATHAN W. McCUTCHEON MORGAN, LEWIS & BOCKIUS LLP
6		
7		By
8		Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
10	Dated: December, 2003	MARK KRIETZMAN
11	·	MARK KRIETZMAN CHRISTOPHER DARROW VALERIE W. HO GREENBERG TRAURIG LLP
12		GREENBERG TRAURIGELF
13		ByMark Krietzman
14	·	Mark Krietzman Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December 23, 2003	TERESA M. CORBIN
16	•	GLENN W. RHODES CHRISTOPHER A. MATHEWS
17		BRIAN S. Y. KIM HOWREY SIMON ARNOLD & WHITE LLP
18		P Clint - 1. A Made alock
19		By Christopher A. Mathews / BSK Christopher A. Mathews
20		Attorneys for Defendants/Counterclaimants CHUNGHWA PICTURE TUBES, LTD., JEAN COMPANY, LTD., LITE-ON TECHNOLOGY
21		CORPORATION, LITE-ON TECHNOLOGY INTERNATIONAL INCORPORATED, TPV
22		TECHNOLOGY LTD. and ENVISION
23	7. 1. 7.	PERIPHERALS, INC.
24	Dated: December, 2003	SCOTT R. MILLER TRACY R. ROMAN
25		BINGHAM McCUTCHEN LLP
26		By
27		Scott R. Miller Attorneys for Defendant VIEWSONIC
28		CORPORATION

C	ase 1:06-cv-00726-JJF Document	389-9 Filed 08/12/2008 Page 9 of 108
1	to meet and confer to reduce the n	umber of claims asserted and to reduce the
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3	Dated: December, 2003	JEFFREY N. BROWN
4		TERESA A. MACDONALD ANN A. BYUN
5		ANTHONY C. ROTH NATHAN W. McCUTCHEON
6	·	MORGAN, LEWIS & BOCKIUS LLP
7		Ву
8		Jeffrey N. Brown Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
9	Dotadi Docombon 2002	•
10	Dated: December, 2003	MARK KRIETZMAN CHRISTOPHER DARROW
11		VALERIE W. HO GREENBERG TRAURIG LLP
12		Dec
13		Mark Krietzman
14		Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December, 2003	TERESA M. CORBIN
16	·	GLENN W. RHODES CHRISTOPHER A. MATHEWS BRIAN S. Y. KIM
17		HOWREY SIMON ARNOLD & WHITE LLP
18		D.,
19		Christopher A. Mathews
20		Attorneys for Defendants/Counterclaimants CHUNGHWA PICTURE TUBES, LTD., JEAN
21		COMPANY, LTD., LITE-ON TECHNOLOGY CORPORATION, LITE-ON TECHNOLOGY INTERNATIONAL INCORPORATED, TPV
22	·	TECHNOLOGY LTD. and ENVISION PERIPHERALS, INC.
23	Dated: December 23, 2003	SCOTT R. MILLER
24	, , , , , , , , , , , , , , , , , , , ,	TRACY ROMAN BINGHAM McCUTCHEN LLP
25 26		(Innels
20 27		By Scott R. Miller
27 28		Attorneys for Defendant VIEWSONIC CORPORATION
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EXHIBIT C

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT C U.S. Patent No. 4,624,737

CI AIM TERMS	AGREED CONSTRUCTION
"surface passivation film"	A thickness of material that provides protection such as
	electrical stability and chemical isolation.
"insulating substrate"	The material (such as glass, quartz, ceramic,
	insulator-coated silicon or insulator-coated metal) upon
	which the transistor is fabricated to provide mechanical
	support and electrical insulation.
"on said gate electrode and	Above and supported by or in contact with the gate
substrate"	electrode and the insulating substrate.
"them"	The gate insulating film, the high-resistivity semiconductor
	film, and the conducting film containing at least the low-
	resistivity semiconductor film.

EXHIBIT D

	1	_			<u>) </u>					tΛ		<u> </u>			_	-							
Defendants' Support	Intrinsic Evidence:	/3/ Fateut, col. 1 lines 6-14; col. 2 line	61 - col. 2 line 2; col.	2 lines 8-10; col. 3	lines 22-24.		Extrinsic Evidence:	"Thin film	technology" for	circuits and systems is	defined as "a	technology in which a	thin film (a few	hundred to a few	thousand angstroms in	thickness) is applied	by vacuum deposition	to an insulating	substrate." IEEE	Standard Extrinsic	Evidence of Electrical	and Electronic Terms	939 (3rd ed. 1984)
Defendants' Construction	A semiconductor	current flow between	source electrode and	drain electrode is	controlled by an	electric field that	penetrates the	semiconductor; this	field is introduced by	a voltage applied at	the gate electrode,	which is separated	from the	semiconductor by an	insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate.	,			
LPL's Support	Intrinsic Evidence:	lines 6-29, 56-58, 61-	68; col. 2, lines 1-2, 8-	68; col. 3, lines 1-62;	col. 4, lines 1-23;	Figs. 1a-3d; and	claims 1-4. (LPL Exh.	1)		'737 patent discloses	various techniques for	fabricating thin films,	such as chemical	vapor deposition	(CVD) (e.g., 2:24-33),	sputtering (2:33-36),	molecular beam	deposition (4:19-20),	ion beam deposition	(4:19-20).		"Any suitable means	of applying the
LPL's Construction	A three-terminal	in which the current	flow through one pair	of terminals, the	source and drain, is	controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	a voltage applied at	the third terminal, the	gate, which is	separated from the	\sim	insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate	rather than in a single	crystal silicon wafer.
Claim Term	thin-film transistor																						

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D U.S. Patent No. 4,624,737

Defendants' Support	("1984 IEEE"), Exh.	1		"A thin-film	transistor, TFT,	fabricated by	evaporation of all	components on to an	insulating substrate	has been developed"	Paul K. Weimer, The	TFT – A New Thin-	Film Transistor in 49	Proceedings of the	IRE 1462-64 (1962),	Exh. 2.		<u>}</u>						
Defendants' Construction		,		-				,								,								
LPL's Support	various films	throughout this	procedure in the	vacuum may be	employed such as, for	example, evaporation,	sputtering, and the	like."	USPN 4,331,758 to	Luo issued May 25,	1982, col. 4, lines 11-	14 (LPL Exh. 2).		"A thin-film transistor	(TFT) is an insulated	grid field effect	transistor. It is similar	to a MOS transistor	(metal-oxide	semiconductor) with	the difference that it is	produced on an	amorphous substrate	
LPL's Construction																								
Claim Term				-																				

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Defendants' Support																	_							
Defendants' Construction												-												
LPL's Support	monocrystalline	silicon wafer. As they	are not limited by the	size of the crystalline	substrate, TFT circuits	can have very large	dimensions. The TFT	on an insulating	substrate has been	investigated in three	different ways"	USPN 4,426,407 to	Morin et al. issued	Jan. 17, 1984, col. 1,	lines 13-22 (emphasis	added) (LPL Exh. 3).	, ,	Extrinsic Evidence:	The Penguin	Dictionary of	Electronics 569 (3rd.	ed. 1998) ("1998	Penguin") ("thin-film	transistor (TFT) A
LPL's Construction							_																	
Claim Term					,																			

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Defendants' Support				-										** **********************************										
Defendants' Construction																								
LPL's Support	MOSFET that is	fabricated using thin-	film techniques on an	insulating substrate	rather than on a	semiconductor chip.")	(LPL Exh. 4); id. at	205-207 ("field-effect	transistor (FET) It	is a three terminal	semiconductor device	in which the current	flow through one pair	of terminals, the	source and the drain,	is controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	the voltage applied at	the third terminal, the	gate"); id. at 70
LPL's Construction																						-		
Claim Term																								

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		("chin A emoll	Construction	
		piece of single crystal		
		of semiconductor		
		material containing		
		either a single		
		component or device		
		or an integrated		
		circuit.").		
		See also The Penguin		
		Dictionary of		
		Electronics, 71, 186-		
		192, 583 (2nd. ed.		
		1988) ("1988		
		Penguin") (LPL Exh.		
		5).		
	A patterned,	Intrinsic Evidence:	A conductive element	Intrinsic Evidence:
	electrically conductive	"FIG. 2a shows in a	of a single thin-film	"Metals such as Cr,
	material that controls	sectional view the	transistor that controls	Mo, W, Al, Ta, etc.,
	current flow through	initial step for	the current between	and their silicides,
	the channel between	selectively forming a	source and drain by a	impurity-doped
	the source electrode	gate electrode 2 on an	voltage applied to its	polysilicon and other
	and drain electrode.	insulating substrate 1.	terminal. The pate	like materials can be

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Defendants' Support	used as said gate	electrode 2." '737	Patent, col. 2 lines 14-	16.		"FIG. 3a illustrates a	step in which gate	electrode 2 extending	along one line and	gate electrodes 2' on	another line are	formed on a	transparent insulating	substrate 1 such as	glass substrate." '737	Patent, col. 3 lines 26-	28. See also Figs. 1-3; 1	Col. 1 lines 15-17;	,	Extrinsic Evidence:	"Gate" is defined as a	structural element of a	TFT that "controls the	current between
Defendants' Construction	electrode is distinct	from the gate line and	the gate pad associated	with the gate	electrode.						•													
LPL's Support	Metals such as Cr,	Mo, W, Al, Ta, etc.,	and their silicides,	impurity-doped	polysilicon and other	like materials can be	used as said gate	electrode 2." '737	Patent at col. 2, lines	7-16.		"FIG. 3a illustrates a	step in which gate	electrode 2 extending	along one line and	gate electrodes 2' on	another line are	formed on a	transparent substrate 1	such as a glass	substrate," '737	Patent at col. 3, lines	22-29.	
LPL's Construction												-								-				
Claim Term																								

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Defendants' Support	source and drain by a voltage applied to its terminal." 1984 IEEE 384, Exh. 1.	U.S. Patent No. 4,331,758 to Luo, Figures 8 and 8A, col. 7 line 17 to col. 8 line 9, Exh. 15.	"Gate" is defined as "[a]n electrode or electrodes in a field- effect transistor." See The Penguin Dictionary of Electronics, 237 (2nd. ed. 1988) ("1988 Penguin"), Exh. 18.	"[A] gate insulating
Defendants' Construction				Successively depositing each
LPL's Support	See also Figs. 1-3; and claim 1.			"[A]s shown in FIG.
LPL's Construction	·			The formation of the gate insulating film,
Claim Term				continuously depositing

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Defendants' Support	resistivity film 4, a	low-resistivity a-Si:H	(usually hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode	2 and substrate 1	without exposing them	to an oxidizing	atmosphere. Such	successive deposition	can be accomplished,	for instance, by	forming [films 3, 4	and 20] in the same	evacuated chamber in	a plasma CVD	apparatus. It is also	possible to form said	films successively in
Defendants' Construction	of the underlying film	or structure without	interruption and	without performing	any processing steps	between the	deposition of each	constituent film.		•														
LPL's Support	film 3 (such as silicon	nitride film) and an	amorphous silicon	film 4 are	continuously	deposited" '737	Patent at col. 1, lines	17-21.		"In the next step	illustrated in FIG. 2b	in a sectional view, a	gate insulating film 3,	a high-resistivity film	4, a low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode
LPL's Construction	semiconductor film	and conducting film	without intervening	films.							-													
Claim Term															-									

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Defendants' Support	the respective	chambers by using a	plasma CVD	apparatus having in-	line chambers.	Further, when a	sputtering or	metalizing chamber is	additionally provided,	conducting film 30	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent, col. 2 lines 17-	36.		See also '737 Patent	Col. 1 lines 17-21, 32-	54; col. 3 lines 28-35,	53-62; col. 4 lines 1-	13; Abstract.		Extrinsic Evidence:
Defendants' Construction																						•		
LPL's Support	2 and substrate 1	without exposing them	to an oxidizing	atmosphere. Such	successive deposition	can be accomplished,	for instance, by	forming [films 3, 4,	and 20] in the same	evacuated chamber in	a plasma CVD	apparatus. It is also	possible to form said	films successively in	the respective	chambers by using a	plasma CVD	apparatus having in-	line chambers.	Further, when a	sputtering or	metalizing chamber is	additionally provided,	conducting film 30
LPL's Construction			715																					
Claim Term																			:					

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D U.S. Patent No. 4,624,737

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Defendants' Support	"Continuous" is	defined as "marked by	uninterrupted	extension in space,	time, or sequence."	1981 Webster's 243-	44, Exh. 3.		"Continuous" is	defined as "extending	or prolonged without	interruption or	cessation; unceasing,"	The American	Heritage Dictionary	317 (2d College Ed.	1985), Exh. 16.		W.E. Spear & P.G.	LeComber.,	Fundamental and	Applied Work on	Glow Discharge	Material, in The
Defendants' Construction																								
LPL's Support	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent at col 2, lines	17-37. See also '737	Patent at col. 3, lines	28-35, 54-62; col. 4,	lines 1-13; Abstract;	Figs. 2b and 3b; and	claims 1 and 2.		Extrinsic Evidence:	The American	Heritage College	Dictionary 1215 (2d	College Ed. 1985)	("1985 American	Heritage Dictionary")	(defining "successive"	as "[f]ollowing in an	uninterrupted order or	sequence.") (LPL Exh.	6); id. at 317 (defining
LPL's Construction																								
Claim Term																								

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D U.S. Patent No. 4,624,737

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		"continuous" as	COURT MOTION	Dhysion of
		contained as		r nystes of
		extending or		Hydrogenated
		prolonged without		Amorphous Silicon I,
		interruption or		Chapter 3 64-68 (J.D.
		cessation;		Joannopoulos and G.
		unceasing").		Lucovsky eds.,
				Springer-Verlag 1984)
		The American		("1984 Spear")
		Heritage College		(describing vacuum
		Dictionary 301 (3d		deposition systems),
		College Ed. 1997)		Exh. 4.
	٠	(defining "continuous"		
		as "uninterrupted in		P.G. LeComber &
		time, sequence,		W.E. Spear, The
		substance, or extent")		Development of the a-
		(LPL Exh. 7).		Si:H Field Effect
				Transistor and its
		1981 Webster's 243-		Possible Applications,
		44 (defining		in 21D
		"[c]ontinuous" as		Semiconductors and
		"marked by		Semimetals 89-95
		uninterrupted		(1984) ("1984
		extension in space,		LeComber")
		time, or sequence.")		(describing single and

)				<u> </u>			
Defendants' Support	multi-chamber deposition systems). Exh. 5.	T. Kodama et al., A Self-Alignment Process for	Amorphous Silicon Thin Film Transistors,	3-7 IEEE Electron Device Letters 187-89 (Jul. 1982) ("1982	Kodama") (describing a continuous denosition process).	Exh. 6. Japanese patent	publication JP 56- 135968 to Osada et al.	published October 23, 1981, Figs. 1, 2; Cols. 7-31 (describing	continuous deposition
Defendants' Construction									
LPL's Support	(Defendant's Exh. 3.)								
LPL's Construction									
Claim Term									-

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Defendants' Support	of layers). Exh. 7.	U.S. Patent No.	4,331,758 to Luo, Col.	1, Lines 9-54, Exh. 15.	Intrinsic Evidence:	'737 Patent, Figs. 1-3;	Col. 1 lines 17-21; col.	2 lines 17-32, 36-38;	col. 3 lines 28-35.		Extrinsic Evidence:	"Film" is defined as "a	thin covering or	coating" and "an	exceedingly thin	layer." 1981	Webster's 425, Exh. 3.		"Gate" is defined as a	structural element of a	TFT that "controls the	current between	source and drain by a
Defendants' Construction					A thickness of	material (such as	SiNx) that has high	electrical resistance	and insulates the gate	electrode from the	transistor	semiconductor.		-									
LPL's Support					Intrinsic Evidence:	"Such successive	deposition can be	accomplished, for	instance, by forming a	silicon nitride (SiNx)	film as gate insulating	film 3 from a mixed	gas of SiH, and NH3,	", '737 Patent at	col. 2, lines 24-26.		"[A] multi-layer film.	can be used as said	gate insulating film	3." '737 Patent at col.	2. lines 36-38.		See also '737 Patent at
LPL's Construction					A thickness of	material (such as	SiNx) that has high	electrical resistance	and insulates the	transistor gate from at	least the transistor	semiconductor.											·
Claim Term					gote inculating film	gate mount mm													-				

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Defendants' Support	voltage applied to its	terminal." 1984 IEEE	384, Exh. 1.		"Insulating material"	is defined as "a	substance or body, the	conductivity or which	is zero or, in practice,	very small." 1984	<i>IEEE</i> 447, Exh. 1.		"Layer" is defined as a	"thickness, coating, or	stratum spread out or	covering a surface."	1985 American	Heritage Dictionary	719, LPL Exh. 6.				Intrinsic Evidence:	"Such successive
Defendants' Construction																						-	A thickness of	semiconductor with no
LPL's Support	1:12-21, 2:18-38,	3:28-35; Abstract;	Figs. 1b-1d, 2b-2e,	and 3b-3d; and claim	1	-	Extrinsic Evidence:	1988 Penguin at 194	(defining "film" as a	"coating with a	minimal thickness	dimension.") (LPL	Exh. 5).		1985 American	Heritage Dictionary at	719 (defining "layer"	as a "thickness,	coating, or stratum	spread out or covering	a surface.") (LPL Ex.	6).	Intrinsic Evidence:	"Such successive
LPL's Construction																							A thickness of	semiconductor
Claim Term													-						-				high-resistivity	semiconductor film

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737

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Defendants' Support	deposition can be	accomplished, for	instance, by	forming a high-	resistivity a-Si:H film	4 by using SiH ₄ in	the same evacuated	chamber in a plasma	CVD apparatus."	'737 Patent, col. 2	lines 23-29.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,	for instance, SiF ₄ , or a	microcrystalline	amorphous silicon
Defendants' Construction	intentionally added	impurities to increase	its conductivity,	resulting in an	electrical resistance	many orders of	magnitude higher than	a low-resistivity	semiconductor film.															
LPL's Support	deposition can be	accomplished, for	instance, by	forming a high-	resistivity a-Si:H film	4 by using SiH ₄ and	forming a n ⁺ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4	in the same evacuated	chamber in a plasma	CVD apparatus."	'737 patent at col. 2,	lines 23-29.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,
LPL's Construction	material (such as	amorphous silicon,	hydrogenated	amorphous silicon,	amorphous silicon-	fluorine alloy,	amorphous silicon-	hydrogen-fluorine	alloy, or a	microcrystalline	amorphous silicon)	that has a higher	resistance to current	flow relative to the	low-resistivity	semiconductor film	(later recited in the	claim).	٠					
Claim Term																								

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Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		for instance, SiF4, or a		film." '737 Patent.
		microcrystalline		col. 2 lines 38-43.
,		amorphous silicon		
		film." '737 patent at		See also '737 Patent,
		col. 2, lines 38-43.		Figs. 1-3; col. 1 lines
				8-11, 17-32; col. 2
		See also '737 Patent at		lines 17-32; col. 3
		col. 1, lines 8-29, 32-		lines 28-35.
		46, col. 2, lines 17-32,		
		38-43, 54-60; col. 3,		Extrinsic Evidence:
		lines 7-10, 16-21, 28-		Shyh Wang, Solid
		41, 48-62; col. 4, lines		State Electronics 129,
		1-23; Abstract; Figs.		155 (McGraw Hill
		1b-1d, 2b-2e, and 3b-		1966) ("1966 Wang")
		3d; and claims 1 and		(describing relative
		2.		properties of
				conductors,
		Extrinsic Evidence:		semiconductors and
		1988 Penguin at 131		insulators), Exh. 8
	,	(defining "doping		
		level" as a "[t]he		P.G. LeComber,
	•	amount of doping		Doping and the
		necessary to achieve		Density of States of
		the desired		Amorphous Silicon, in

						})						
Defendants' Support	Fundamental Physics	of Amorphous	Semiconductors 46-55	(F. Yonezawa ed.,	Springer-Verlag 1981)	("1981 LeComber")	(comparing doped and	nndoped	semiconductors), Exh.	6		1984 Spear 91-97	(comparing doped and	nndoped	semiconductors), Exh.	4.	See also 1984	LeComber 89-95, Exh.	5; K.D. MacKenzie et	al., The	Characteristics and	Properties of	Optimised Amorphous
Defendants' Construction																٠							
LPL's Support	characteristic in a	semiconductor. Low	doping levels give	a high-resistivity	material; high doping	levels give a low-	resistivity material.")	(LPL Exh. 5).		Id. at 194 (defining	"film" as a "coating	with a minimal	thickness dimension.")										
LPL's Construction																							
Claim Term												-						•					

LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		Construction	•
			Silicon Field Effect
			Transistors, in A31
			Applied Physics A,
			Solids and Surfaces
			87-88 (1983) ("1983
			MacKenzie"). Exh.
			.01
			"Layer" is defined as a
•			"thickness, coating, or
			stratum spread out or
			covering a surface."
			1985 American
			Heritage Dictionary
			719, LPL Exh. 6.
A thickness of	Intrinsic Evidence:	A thickness which	Intrinsic Evidence:
lly conductive	Claim 1 of the '737	includes a material	"[A] conducting film
material.	patent, which recites	consisting of an	30 made of a metal or
	"a conducting film	elemental metal, metal	other material" '737
	containing at least a	alloy, or film of	Patent, Col. 2 lines 17-
	low-resistivity	optically transparent	23.
<u></u>	semiconductor film."	material, and having	
		an electrical resistance	"Further, when a
	Claim 2 of the '737	several orders of	Sputtering or

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
	-		Construction	
		patent, which recites	magnitude lower than	metalizing chamber is
		"said conducting film	a low-resistivity	additionally provided,
		is composed of at least	semiconductor film.	conducting film 30
		two layers consisting		can be also deposited
		of a low-resistivity		continuously without
		semiconductor film		exposure to the
		and thereon a		atmosphere." '737
	-	refractory metal film		Patent, col. 2 lines 32-
		or transparent		36.
		conducting film."		
				"As said conducting
		"In this example, no		film 30, it is desirable
		conducting film is		to use a stable
-		formed on low-		conducting film such
		resistivity amorphous		as a transparent
		silicon film 20, but a		conducting film made
		conducting film such		of a refractory metal
		as ITO film may be		such as Cr, W, Mo,
		formed on said low-		Ta, etc., and silicides
		resistivity film 20 as		thereof, or indium-tin-
		in the example shown		oxide (ITO), SnO ₂ and
		in FIG. 2." '737		the like. Use of a
		patent at col. 3, lines		transparent conducting
		48-52.		film has the advantage

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				that the process is
		"In the next step		simplified when the
		illustrated in FIG. 2b		thin-film transistor of
		in a sectional view, a		this invention is
,		gate insulating film 3,		applied to an active
		a high-resistivity film		matrix liquid crystal
		4, a low-resistivity a-		display." '737 Patent,
		Si:H (usually		col. 2 lines 46-53.
		hydrogenated		
		amorphous silicon)		"The same materials
		film 20 and a		as used for conducting
	-	conducting film 30		film 30 and other
		made of a metal or		materials such as Al
		other material are		can be used for said
,		successively formed		drain and source
		on said gate electrode	-	electrode members 15,
		2 and substrate 1"		16." '737 Patent, col.
		'737 patent at col. 2,		3 lines 4-7.
		lines 17-23.		
				win this example, no
		"As said conducting		conducting film is
		film 30, it is desirable		formed on low-
		to use a stable		resistivity amorphous
		conducting film such		silicon film 20, but a

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		as a transparent		conducting film such
		conducting film made		as ITO film may be
		of a refractory metal		formed on said low-
,		such as Cr, W, Mo,		resistivity film 20 as
		Ta, etc., and silicides		in the example shown
		thereof, or indium-tin-		in FIG. 2." '737
		oxide (ITO), SnO ₂ and		Patent, col. 3 lines 48-
		the like." '737 patent		52.
		at col. 2, lines 46-50.		
				"The same is true with
		See also '737 Patent at		the interface of low-
,		col. 1, lines 25-29, 32-		resistivity amorphous
		51, col. 2, lines 10-36,		silicon film 20 and
•		43-68; col. 3, lines 1-		conducting film 30.
		10, 28-35, 48-62; col.		Further, since the
		4, lines 1-23; Abstract;		interfaces of low-
	,	Figs. 2b-2e and 3b-3d.		resistivity amorphous
				silicon film 20 or
		"Deposition of a		conducting film 30
		metallic grid coating		and drain and source
		24, e.g. of highly		electrodes 15, 16 can
		doped silicon or		be cleaned" '737
		aluminum (by CVD-		Patent, col. 3 line 57 –
		plasma) on the entire		col. 4 line 2.

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						<u>/</u>)						
Defendants' Support		See also '737 Patent,	Figs. 1-3; col. 2 lines	54-60.		Extrinsic Evidence:	"Electrically	conductive materials	that can be prepared	by CVD comprise	elemental metals,	metal alloys,	superconductive	compounds, and films	of optically	transparent	conductors." Thin	Film Processes 315-	317 (J.L. Vossen &	W. Kern eds.,	Academic Press 1978,	Exh. 11.		See also 1966 Wang
Defendants' Construction																								
LPL's Support	surface of the	sample(g)." USPN	4,426,407 to Morin et	al. issued Jan. 17,	1984, col. 3, lines 50-	52 (LPL Exh. 3).		" wherein the	conductive coating is	of highly doped	silicon and is obtained	by reactive gaseous	phase plasma." Id. at	claims 5. See also id.	at claims 1, 3, and 4.		Extrinsic Evidence:	1985 American	Heritage Dictionary at	307 (defining	"conduct[ing]" as	"serv[ing] as a	medium or channel for	conveying") (LPL Ex.
LPL's Construction																								
Claim Term															,									

Defendants' Support	129, 155, Exh. 8; 1984 Spear 91-97, Exh. 4.	See also support cited	by LPL for the term "conducting film".																
Defendants' Construction																			
LPL's Support	6).	1988 Penguin at 194 (defining "film" as a	"coating with a minimal thickness	dimension.") (LPL	Exh. 5).	CRC Handbook of	Chemistry and Physics	12-96 (75th ed., 1994-	1995) (discussing the	resistivity of	semiconducting	minerals) (LPL Exh.	9).	Thin Film Processes	316-317 (J.L. Vossen	& W. Kern eds.,	Academic Press 1978,	(noting that "[t]hin	films of optically
LPL's Construction																-			
· Claim Term							-												

)											<u>)</u>						
Defendants' Support		Intrinsic Evidence:	"[A] low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 are	successively formed	Such successive	deposition can be	accomplished, for	instance, by	forming a n+ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4 in	the same evacuated	chamber in a plasma	CVD apparatus"
Defendants' Construction		A thickness of	semiconductor having	intentionally added	impurities to increase	its conductivity,	resulting in an	electrical resistance	many orders of	magnitude lower than	a high-resistivity	semiconductor film.						
LPL's Support	transparent and electrically conductive materials", including SnO ₂ , are "usually classified" as semiconductors) (Defendants' Exh. 11).	Intrinsic Evidence:	"In the next step	illustrated in FIG. 2b	in a sectional view, a	gate insulating film 3,	a high-resistivity film	4, a low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode	2 and substrate 1
LPL's Construction		A thickness of	semiconductor	material (such as low-	resistivity amorphous	silicon, hydrogenated	amorphous silicon,	amorphous silicon-	fluorine alloy,	amorphous silicon-	hydrogen-fluorine	alloy, or a	microcrystalline	amorphous silicon,	which contains	phosphorous or other	impurities to enhance	the conductivity of the
Claim Term		low-resistivity	semiconductor film								-							

)			-								_	<u>) </u>						
Defendants' Support	'737 Patent, col. 2	11163 17-32.	"Such alloys [a-Si:F	or a-Si:H:F alloy	using, for instance,	SiF ₄ , or a	microcrystalline	amorphous silicon	film] can be also used	for said low-resistivity	amorphous silicon	film 20, and such film	may contain other	impurites beside	phosphorous	impurities." '737	Patent, col. 2 lines 38-	45.		"In this example, no	conducting film is	formed on low-	resistivity amorphous
Defendants' Construction																					• .		
LPL's Support	without exposing them	to an oxidizing	successive deposition	can be accomplished,	for instance, by	forming a n ⁺ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4	.," '737 patent at col.	2, lines 17-30.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,	for instance, SiF4, or a	microcrystalline	amorphous silicon
LPL's Construction	film) that has a lower	resistance to current	liow fetalive to une high-resistivity	semiconductor film.																-			
Claim Term																							

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						<u>) </u>											_	<u>)</u>						
Defendants' Support	silicon film 20, but a	conducting film such	as ITO film may be	formed on said low-	resistivity film 20 as	in the example shown	in FIG. 2." '737	Patent, col. 3 lines 48-	52.		"The same is true with	the interface of low-	resistivity amorphous	silicon film 20 and	conducting film 30.	Further, since the	interfaces of low-	resistivity amorphous	silicon film 20 or	conducting film 30	and drain and source	electrodes 15, 16 can	be cleaned" '737	Patent, col. 3 line 57 –
Defendants' Construction																								
LPL's Support	film. Such alloys can	be also used for said	low-resistivity	amorphous silicon	film 20, and such film	may contain other	impurities beside	phosphorous	impurities." '737	patent at col. 2, lines	38-50.		See also '737 Patent at	col. 1, lines 25-29,	32-51; col. 2, lines 17-	45, 54-68; col. 3, lines	1-10, 28-41, 48-62;	col. 5, lines 1-23;	Abstract; Figs. 1d; 2b-	2e, and 3b-3d; and	claims 1 and 2.		Extrinsic Evidence:	1988 Penguin at 131
LPL's Construction											,													
Claim Term																								

is' Defendants' Support	on	col. 4 line 2.		See also '737 Patent,	Figs. 1-3; Col. 1 lines	8-11, 17-32; col. 2	lines 32-36, 46-60;	col. 3 lines 4-7.		Extrinsic Evidence:	1984 Spear 91-97.	Exh. 4; 1984	LeComber 89-95, Exh.	5; 1966 Wang 129,	155, Exh. 8; 1981	LeComber 46-55, Exh.	9; 1983 MacKenzie	87-88. Exh. 10.		"Layer" is defined as a	"thickness, coating, or	stratum spread out or	covering a surface."	1985 American	
Defendants'	Construction							-																	
LPL's Support		(defining "doping	level" as a "[t]he	amount of doping	necessary to achieve	the desired	characteristic in a	semiconductor. Low	doping levels give	a high-resistivity	material; high doping	levels give a low-	resistivity material.")	(LPL Exh. 5).		Id. at 194 (defining	"film" as a "coating	with a minimal	thickness	dimension.").					
LPL's Construction		-																							
Claim Term												,			,										

t			- 8	·		,						_		 	·	_	· s						
Defendants' Support	719, LPL Exh. 6.	Intrinsic Evidence:	"[A] low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	'737 Patent, col.	2 lines 17-23.	In this example, no	conducting film is	formed on low-	resistivity amorphous	silicon film 20, but a	conducting film such	as ITO film may be	formed on said low-	resistivity film 20 as	in the expense of the
Defendants' Construction		A conducting film	with an adjoining thin	layer of low-resistivity	semiconductor and	possibly other	adjoining layers.																
LPL's Support		Intrinsic Evidence:	Claim 2 of the '737	patent, which recites	"said conducting film	is composed of at least	two layers consisting	of a low-resistivity	semiconductor film	and thereon a	refractory metal film	or transparent	conducting film."	Compare '737 patent	at col. 3, lines 40-	41("exposed portion	of low-resisitivity	amorphous silicon	film 20 is removed"),	Figs. 2d and 3c with	Claim I ("a fifth step	for selectively	Total Service
LPL's Construction		The conducting film is	composed of a low-	resistivity	semiconductor film	and possibly other	conductive films.																
Claim Term		conducting film	containing at least a	low-resistivity	semiconductor film																		

LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		Construction	
	conducting film		in FIG. 2." '737
	exposed on said island		Patent, col. 3 lines 48-
	region").		52.
		•	
	Claim 1 ("a third step		"The same is true with
	in which said high		the interface of low-
	resistivity		resistivity amorphous
	semiconductor film		silicon film 20 and
	and said conducting		conducting film 30.
	film are selectively		Further, since the
	etched") (note no		interfaces of low-
	separate mention is		resistivity amorphous
	made of low		silicon film 20 or
	resistivity		conducting film 30
	semiconductor film).		and drain and source
			electrodes 15, 16 can
	See also '737 patent at		be cleaned". '737
	col. 1, lines 18-36, 43-		Patent, col. 3 line 57 –
	57; col. 3, lines 28-41,		col. 4 line 2.
	48-62; col. 4, lines 1-		
,	12; Figs 2b-2e, 3b-3d;		"A gate insulating
	claim 1.	-	film, a high-resistivity
			semiconductor film, a
	" wherein the		low-resistivity

Defendants' Support	semiconductor film	and if necessary a	conducting film are	successively deposited	in lamination".	'737 Patent, Abstract		See also '737 Patent,	Figs. 2b-2e; Claim 2;	Col. 2 lines 23-33, 43-	54; col. 3 lines 4-7.	Extrinsic Evidence:	"Contain" is defined	as "to have within,"	"comprise" or	"include." 1981	Webster's 242, Exh. 3.		"Include" is defined as	"to take in or comprise	as part of a larger	aggregate or	principle." 1981
Defendants' Construction																							
LPL's Support	conductive coating is	of highly doped	silicon and is obtained	by reactive gaseous	phase plasma." USPN	4,426,407 to Morin et	al. issued Jan. 17,	1984, claim 5 (LPL	Exh. 3). See also id.	col. 3, lines 50-52;	claims 1, 3, and 4.	Extrinsic Evidence:	1985 American	Heritage Dictionary at	315-316 (defining	"contain" as "to have	as component parts;	comprise; include")	(LPL Exh. 6).	-	1988 Penguin at 93	(defining "conductor"	as a "[a] material that
LPL's Construction								.,										<u> </u>					
Claim Term																							

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		offers a low resistance		Webster's 576, Exh. 3.
		to the passage of		
		electrical current:		"Conducting material"
		when a potential		is defined as "a
		difference is applied		conducting medium in
		across it a relatively		which the conduction
		large current flows.")		is by electrons, and
	-	(LPL Exh. 5).		whose temperature
				coefficient of
		<i>Id.</i> at 131 (defining		resistivity is, except
		"doping level" as a		for certain alloys,
		"[t]he amount of		nonnegative at all
		doping necessary to		temperatures below
		achieve the desired		the melting point."
		characteristic in a		1984 IEEE 175, Exh.
		semiconductor. Low		1.
		doping levels give		
		a high-resistivity		"Semiconductor" is
		material; high doping		defined as "an
		levels give a low-		electronic conductor
		resistivity material.").		with resistivity in the
				range between metals
				and insulators, in
				which the electric-

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Defendants' Support	charge-carrier	increases with	increasing temperature	over some temperature	815, Exh. 1.	See also 1983	MacKenzie 87-88.	Exh. 10; Japanese	patent publication JP	58-190061 to Aoki et	al. published	November 5, 1983,	Figs 4, 5; Cols. 7-9.	Exh. 12	 Layer 18 defined as a	"thickness, coating, or	stratum spread out or	covering a surface."	1985 American	Heritage Dictionary
Defendants' Construction											•									
LPL's Support																				
LPL's Construction								,									•			
Claim Term																				

Defendants' Support	719, LPL Exh. 6.	See support for claim	term without	exposing them to an	oxidizing atmosphere"	below.				_											_			
Defendants' Construction		An atmosphere that	would create all oxide	on a film.																		·		
LPL's Support		Intrinsic Evidence:	in the conventional	process shown in	FIGS. 1a to 1d, since	the masking step	precedes the	deposition of n+	amorphous films 25,	26, natural oxide is	produced on the	exposed surface of	amorphous silicon	film 4. Although such	natural oxide can be	removed by an	aqueous solution of	hydrofluoric acid (HF)	or a similar substance,	the possibility is still	great that oxygen and	its compounds as well	as other impurities can	collect on the laminate
LPL's Construction		An atmosphere that	would create	substantial oxidation	on a film.											-		,					5	
Claim Term		oxidizing atmosphere																						

Defendants' Support															,								
Defendants' Construction												-											
LPL's Support	surface as it is	exposed to the	atmosphere. This	would give rise to	electrical resistance	between the source	and drain and between	channels in the thin-	film transistor thus	obtained, making such	transistor unable to	exhibit its desired	characteristics." '737	patent at col. 1, lines	32-44.	"As described above,	according to the	present invention, no	oxides, etc., are	formed at the interface	of high-resistivity	amorphous silicon	film 4 and low-
LPL's Construction																							
Claim Term																						-	

Defendants' Support																		-						
Defendants' Construction																,								
LPL's Support	resistivity amorphous	silicon film 20, so that	a good junction can be	formed. The same is	true with the interface	of low-resistivity	amorphous silicon	film 20 and	conducting film 30.	Further, since the	interfaces of low-	resistivity amorphous	silicon film 20 or	conducting film 30	and drain and source	electrodes 15, 16 can	be cleaned without	damaging the high-	resistivity amorphous	silicon film, a good	contact can be	obtained without	sacrificing the	inherent properties of
LPL's Construction											-				-									
Claim Term																								

					 ,)					
Defendants' Support				Intrinsic Evidence: "In the conventional	process shown in	FIGS. 1a to 1d, since the masking step	precedes the	deposition of n+	amorphous films 25,	26, natural oxide is	produced on the
Defendants' Construction				Without permitting the gate insulating film,	high-resistivity	semiconductor film, low-resistivity	semiconductor film, or	conducting film to	come into contact with	an atmosphere that	would create an oxide
LPL's Support	thin-film transistor." '737 patent at col. 3, line 53 – col. 4, line 2. See also '737 Patent at col. 1, lines 21-51; col. 2 lines 17-53; col. 3 lines 28-35 53-62.	col. 4, lines 1-23; Abstract; Figs 2b-2e, 3b-3d; and claims 1	and 2.	Intrinsic Evidence: '737 patent at col. 1,	lines 32-44, 47-53;	col. 2, lines 17-36; col. 3, lines 28-35, 53-	62; col. 4, lines 1-12;	Figs. 2b-2e, 3b-3d;	claims 1 and 2.	. *	
LPL's Construction				This phrase is a combination of	previously defined or	agreed constructions of "them" and	"oxidizing	atmosphere", namely,	the gate insulating	film, the high-	resistivity
Claim Term				without exposing them to an oxidizing	atmosphere						

LPL's Support

LPL's Construction	LPL's Support C	Defendants' Construction	Defendants' Support
	·		exhibit its desired characteristics " '737
			Patent, col. 1, lines
			32-46.
			"[Films 3, 4, 20 and
			30] are successively
			formed on said gate
			electrode 2 and
,			substrate 1 without
			exposing them to an
		,	oxidizing atmosphere.
			Such successive
			deposition can be
			accomplished, for
			instance, by forming
			[films 3, 4 and 20] in
•			the same evacuated
			chamber in a plasma
			CVD apparatus. It is
			also possible to form
			said films successively
			in the respective
			chambere hy neing a

Defendants' Support	plasma CVD	apparatus having in-	line chambers.	Further, when a	sputtering or	metalizing chamber is	additionally provided,	conducting film 30	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent, col. 2 lines 17-	36.		"As described above,	according to the	present invention, no	oxides, etc., are	formed at the interface	of high-resistivity	amorphous silicon	film 4 and low-	resistivity amorphous
Defendants' Construction																								
LPL's Support		-											• • • • • • • • • • • • • • • • • • •	•					,					
LPL's Construction															•									
Claim Term										,	,												,	

Defendants' Support	silicon film 20, so that	a good junction can be	formed. The same is	true with the interface	of low-resistivity	amorphous silicon	film 20 and	conducting film 30."	'737 Patent, col. 3,	line 53-59.		"A gate insulating	film, a high-resistivity	semiconductor film, a	low-resistivity	semiconductor film	and if necessary a	conducting film are	successively deposited	in lamination without	exposing them to any	oxidizing atmosphere	including atmospheric	air," '737 Patent,
Defendants' Construction											·							-						
LPL's Support							-																	
LPL's Construction										-														
Claim Term												٠		,										

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D

U.S. Patent No. 4,624,737

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Intrinsic Evidence:
selected portions of a "Fig. 2c illustrates the
فع
_
etching, and ion film 20 and high-
to resistivity amorphous
produce a desired silicon film 4 are left
pattern on the surface. as an island region by
etching in a single

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737

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Defendants' Support	masking step. Known	etching techniques	plasma etching,	reactive ion etching,	ion etching, etc., can	be used for this step."	'737 Patent, col. 3	lines 54-60.		See also '737 Patent,	Figs. 1-3; Col. 1 lines	17-21, 25-29; col. 2	lines 60-66; col. 3	lines 7-10, 44-48.									
Defendants' Construction																							
LPL's Support	masking step. Known	etching techniques	plasma etching.	reactive ion etching,	etc., can be used for	this step." '737 patent	at col. 2, lines 54-60.		See also '737 Patent at	col. 1, lines 14-21, 25-	29, 32-35; col. 2, lines	10-16, 54-66; col. 3,	lines 7-10, 28-41, 44-	48; col. 4, lines 3-9;	Figs. 1a-1d; 2a-2e; 3a-	3e; and claim 1.		USPN 4,331,758 to	Luo issued May 25,	1982 (compare col. 7,	line 39 – col. 8, line	10 (describing a wet	etch) with col. 5, lines
LPL's Construction																							
Claim Term																							

<u></u>											_	<u> </u>			
Defendants' Support															See support for claim term "island region
Defendants' Construction								·							Defendants contend
LPL's Support	1-27 (describing the use of a non-etching technique for forming	a patterned surface)) (LPL Exh. 2).	Extrinsic Evidence:	"etching Chemical	portions of a surface	in order to produce a	desired pattern on the	Sullace. 1900 Dangiji 170.71 (1 pt	Exh. 5). Cf. id. at	299-300 (defining "lift	off").	USPN 4,404,731 to	Poleshuk issued Sep.	20, 1983 (LPL Exh. 8).	Intrinsic Evidence: "FIG 2c illustrates the
LPL's Construction											·				A discrete portion of
Claim Term														·	island region

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
	semiconductor film	step in which said	be interpreted as part	on said gate
	and conducting film	conducting film 30,	of the phrase "island	electrode" below.
	that is formed by	low-resistivity	region on said gate	
	selective etching.	amorphous silicon	electrode."	
		film 20 and high-		•
		resistivity amorphous		
		silicon film 4 are left		
		as an island region by		
		etching in a single		
		masking step. Known		- 1
		etching techniques		
		such as wet etching,		
		plasma etching,		
		reactive ion etching,		
		ion etching, etc., can		
		be used for this step."		
		'737 patent at col. 2,		
		lines 54-57.		
		See also '737 Patent at		
		col. 2, lines 54-60;		
		col. 3, lines 28-35;		
		Figs. 2c-2e, 3c-3d; and		
		claim 1.		

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					<u>) </u>											_	<u>)</u>				 	
Defendants' Support	Intrinsic Evidence: The '737 patent	drawings show an	island of material with	no other surrounding	material. '737 Patent,	Figs. 2c, 3b.		"FIG. 2c illustrates the	step in which said	conducting film 30,	low-resistivity	amorphous silicon	film 20 and high-	resistivity amorphous	silicon film 4 are left	as an island region by	etching in a single	masking step." '737	Patent, col. 2 lines 54-	57.	See also '737 Patent,	col. 3 lines 28-35.
Defendants' Construction	Portion of the conducting film, low-	resistivity	semiconductor film	and high-resistivity	semiconductor film	which has been etched	around its entire	perimeter into a	separate isolated	region located over the	gate electrode of a	single thin-film	transistor.							-		
LPL's Support	See definitions of "island region" and,	"gate electrode",	supra.	ı															-			
LPL's Construction	This phrase is a combination of	previously defined or	agreed constructions	of "island region",	"on", and "gate	electrode", namely, a	discrete portion of the	high-resistivity	semiconductor film	and conducting film	that is formed by	selective etching. The	discrete portion is	located above and	supported by or in	contact with the gate	electrode.			-		
Claim Term	island region on said gate electrode)																				

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				Extrinsic Evidence:
				"Island" is defined as
				"1: a tract of land
				surrounded by water
				and smaller than a
<u>.</u> -				continent 2:
			·	something resembling
				an island esp. in its
· · ·				isolated or surrounded
·				position". 1981
				Webster's 608. Exh. 3.
				A.J. Snell et al.,
				Application of
			•	Amorphous Silicon
				Field Effect
-				Transistors in
				Addressable Liquid
				Crystal Display
	,			Panels, in 24 Applied
				Physics at 357, 358
				(April 1981), Exh. 17.
selectively forming	Forming a pattern of	Intrinsic Eyidence:	Forming in selected	Intrinsic Evidence:

upport	3s. 1-3; 17; col.	0-66; II;				<u>ıce:</u>	3s. 1-3;	17; col.	0-66;	36-44;											
Defendants' Support	'737 Patent, Figs. 1-3; Col. 1 lines 15-17; col.	2 lines 10-14, 60-66; col. 3 lines 34-41;	Abstract.			Intrinsic Evidence:	'737 Patent, Figs. 1-3;	Col. 1 lines 15-17; col.	2 lines 10-14, 60-66;	col. 3 lines 4-7, 36-44;	Abstract.										
Defendants' Construction	regions only.					Forming a source	electrode and drain	electrode in selected	regions only by	depositing a	conducting film or	other material such as	AI.	٠		•					
LPL's Support	'737 Patent at col. 1, lines 14-17, 25-29;	col. 2, lines 10-36, 60- 68; col. 3, lines 1-10,	24-52; col. 4, lines 3-	9; Abstract; Figs. 1a-	claim 1.	Intrinsic Evidence:	"In the next step	illustrated in FIG. 3c,	a transparent	conducting film such	as ITO film is	deposited; then, drain	electrode 15 and	source electrode 16	which doubles as a	picture cell electrode	are selectively formed	and the exposed	portion of low-	resistivity amorphous	eilicon film 20 is
LPL's Construction	material (for example, by depositing material	and selectively etching portions of the	material away).			The source electrode	and drain electrode are	selectively formed	together.										-		
Claim Term						a fourth step for	selectively forming a	source electrode and	drain electrode							.					

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Defendants' Support			Intrinsic Evidence:	"Thereafter, as	illustrated in FIG. 1d,	for instance n+	amorphous silicon	films 25, 26 and metal	(such as Al) films 15,	16 are deposited and	selectively etched to	form drain and source	electrodes 5, 6,	thereby completing a	thin-film transistor	unit." '737 Patent.
Defendants' Construction			A conductive element	of a single thin-film	transistor formed over	the source region from	which charge carriers	flow into the channel	toward the drain. The	source electrode is	distinct from the	source/data line and	the source/data pad	associated with the	source electrode.	
LPL's Support	removed." '737 Patent at col. 3, lines 36-41. See also '737 Patent at col. 1, lines	21-29, 32-51; col. 2, lines 17-68; col. 3, lines 1-14, 28-62; col. 4, lines 1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d;	Intrinsic Evidence:	"Then, as illustrated in	FIG. 2d in a sectional	view, drain and source	electrode members 15,	16 are selectively	provided, and	conducting film 30	and low-resistivity	amorphous silicon	film 20 shown in FIG.	2c are selectively	removed with said	electrode members 15.
LPL's Construction			A patterned.	electrically conductive	material formed over	the source region.	Current flows through	the channel between	the source electrode	and drain electrode	under control of the	gate electrode.				
Claim Term			source electrode													

<u>.</u>						_	j)						
Defendants' Support		col. 1 lines 25-29.		See also '737 Patent,	Figs 1d, 2d-2e, 3c-3d;	Col. 2 lines 60-66; col.	3 lines 36-41, 57-62.		Extrinsic Evidence:	"Source" is defined as	a device structure	which "contains the	terminal from which	charge carriers flow	into the channel	toward the drain. It	has the potential	which is less attractive	than the drain for the	carriers in the	channel." 1984 IEEE	855, Exh. 1.		"Source" is defined as	"[t]he electrode in a
Defendants'	Construction																								
LPL's Support		16 serving at least as a	part of the mask "	,737 Patent at col. 2,	lines 60-66.		"In the final step	illustrated in FIG. 2e,	a surface passivation	film 8 is deposited,	and the drain and	source electrodes 15,	16 and gate electrode	2 are partly exposed	(not shown)." '737	Patent at col. 3, lines	11-14.		See also '737 Patent at	col. 1, lines 21-29, 32-	51; col. 2, lines 17-68;	col. 3, lines 1-14, 28-	62; col. 4, lines 1-12;	Abstract; Figs. 1d, 2d-	2e, 3c-3d; and claim 1.
LPL's Construction						-					-													·	
Claim Term																									

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Defendants' Support	field-effect transistor	that supplies charge	carriers (holes or	electrons) to the	interelectrode space."	1998 Penguin 532,	Exh. 18.										,							
Defendants' Construction																								
LPL's Support	-	"[A]Il of the source	electrodes 23 in any	column are electrically	connected together	since each source	electrode forms a	portion of the source	bus conductor. By	electrically addressing	any given column	source bus conductor	23 and any given row	gate bus conductor, a	single transistor of the	array can be turned on,	thereby permitting	current to flow from	its source through the	conductive channel of	the semiconductive	material to the	corresponding drain.	This then can be
LPL's Construction																								
Claim Term															-									

4.														$\overline{}$	_							
Defendants' Support														Intrinsic Evidence:	"Thereafter, as	illustrated in FIG. 1d,	for instance n+	amorphous silicon	films 25, 26 and metal	(such as Al) films 15,	16 are deposited and	selectively etched to
Defendants' Construction	·													A conductive element	of a single thin-film	transistor formed over	the drain region into	which charge carriers	flow from the source	into the channel.		•
LPL's Support	utilized to alter the	optical device, such as	a liquid crystal layer,	thus providing an	optical read-out of a	bit of information."	USPN 4,331,758 to	Luo issued May 25,	1982 at col. 7, lines	40-58; col. 8, lines 1-	10 (LPL Exh. 2). See	also id. Figs. 8 and	8A.	Intrinsic Evidence:	"Then, as illustrated in	FIG. 2d in a sectional	view, drain and source	electrode members 15,	16 are selectively	provided, and	conducting film 30	and low-resistivity
LPL's Construction														A patterned,	electrically conductive	material formed over	the drain region.	Current flows through	the channel between	the source electrode	and drain electrode	innder control of the
Claim Term														drain electrode			,					

Defendants' Support	form drain and source	electrodes 5, 6,	thereby completing a	thin-film transistor	unit." '737 Patent,	col. 1 lines 25-29.		See also '737 Patent,	Figs 1d, 2d-2e, 3c-3d;	Col. 2 lines 60-66; col.	3 lines 36-41, 57-62.		Extrinsic Evidence:	"Drain" is defined as a	device structure which	"contains the terminal	into which charge	carriers flow from the	source into the	channel. It has the	potential which is	more attractive than	the source for the	carriers in the
Defendants' Construction													-									-		
LPL's Support	amorphous silicon	film 20 shown in FIG.	2c are selectively	removed with said	electrode members 15,	16 serving at least as a	part of the mask "	'737 Patent at col. 2,	lines 60-66. See also	'737 Patent at col. 1,	lines 21-29, 32-51;	col. 2, lines 17-68;	col. 3, lines 1-14, 28-	62; col. 4, lines 1-12;	Abstract; Figs. 1d, 2d-	2e, 3c-3d; and claim 1.				,				
LPL's Construction	gate electrode.					-																		
Claim Term																								

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Defendants' Support	channel." <i>1984 IEEE</i> 276, Exh. 1.	"Drain" is defined as "[t]he electrode of a field-effect transistor	through which carriers leave the	interelectrode space."	Exh. 18.	Intrinsic Evidence: '737 Patent, Figs. 1d,	2d-2e, 3c-3d; Col. 1	lines 60-66; col. 3	lines 36-41, 57-62.	Extrinsic Evidence:	The verb "contact" is	defined as "to bring	into contact with" and	the noun is defined as
Defendants' Construction						Touching a part of the surface of the island	region.					,		
LPL's Support						Intrinsic Evidence:	'737 Patent at col. 3,	lines 1-2; Figs. 2d-2e;	3c-3d.	Extrinsic Evidence:	1985 American	Heritage Dictionary at	315 (defining	"contact" as a
LPL's Construction						Forming an electrical connection to a part of	the surface of the	Island (Cg101).	,					
Claim Term						contacting a part of the surface of said	island region							

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		connection between two conductors that		"a union or junction of surfaces" or "the
		permits a flow of		junction of two
		current") (LPL Exh.		electrical conductors
		(9):		through which a
				current passes." 1981
				Webster's 242, Exh. 3.
				The noun "contact" is
				defined as "the
				coming together or
	·			touching of two
				objects or surfaces."
				1985 American
				Heritage Dictionary at
				315, LPL Exh. 6.
selectively removing	The removal of	Intrinsic Evidence:	Removing selected	Intrinsic Evidence:
	selected portions of a	"Thereafter, as	regions only.	'737 Patent, Figs. 1-3;
	surface using etching	illustrated in FIG. 1d,		Col. 1 lines 17-21, 25-
	techniques (such as	for instance n+		29; col. 2 lines 60-66;
	wet etching, plasma	amorphous silicon		col. 3 lines 7-10, 44-
	etching, reactive ion	films 25, 26 and metal		48.
	etching, and ion	(such as Al) films 15,		
	etching) or other	16 are deposited and		

Defendants' Support																	-							
Defendants'	Construction																							
LPL's Support		selectively etched to	form drain and source	electrodes 5, 6,	thereby completing a	thin-film transistor	unit." '737 Patent,	col. 1, lines 25-29.	"Then, as illustrated in	FIG. 2d in a sectional	view, drain and source	electrode members 15,	16 are selectively	provided, and	conducting film 30	and low-resistivity	amorphous silicon	film 20 shown in FIG.	2c are selectively	removed with said	electrode members 15,	16 serving at least as a	part of the mask to	form drain electrode 5
LPL's Construction		techniques in order to	produce a desired	pattern on the surface.															-					
Claim Term																								

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Defendants' Support	,																			
Defendants' Construction	·																			
LPL's Support	and source electrode 6." '737 Patent at col.	2, lines 60-66. "[D]rain electrode 15	and source electrode	16 which doubles as a	picture cell electrode	are selectively formed	and the exposed	portion of low-	resistivity amorphous	silicon film 20 is	removed." '737	Patent at col. 3, lines	38-41.	See also '737 Patent at	col. 1, lines 14-29;	col. 2, lines 10-14, 54-	68; col. 3, lines 1-16,	24-52; Abstract; Figs.	1a-1d, 2a-2e, 3a-3d;	and claim 1.
LPL's Construction																				
Claim Term																				

noddne	or claim ource and des least a ask"	
Defendants' Support	See support for claim term "said source and drain electrodes serving as at least a part of the mask" below.	
Defendants' Construction	At least a part of the layer which defines the edges of the selectively removed region.	
LPL's Support	"Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6." '737 Patent at col. 2, lines 60-66.	See also '737 Patent at col. 1, lines 14-29; col. 2, lines 10-14, 54-68; col. 3, lines 1-16,
LPL's Construction	A "mask" is a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to material to be removed.	
Claim Term	at least a part of the mask	

Defendants' Support			Intrinsic Evidence: " [C]onducting film 30 and low-resistivity amorphous silicon
Defendants' Construction			The source and drain electrodes make a significant contribution to
LPL's Support	24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d; and claim 1; USPN 4,331,758 to Luo issued May 25, 1982 at col. 5, lines 37-col. 6, line 7 (LPL Exh. 2). Extrinsic Evidence: 1988 Penguin at 194 (defining "mask" as "A device used to shield selected areas of a semiconductor chip during the manufacture of semiconductor	components and integrated circuits.) (LPL Exh. 5).	See definition of "source electrode", "drain electrode," and "at least a part of the
LPL's Construction			This phrase is a combination of previously defined constructions of
Claim Term			said source and drain electrodes serving as at least a part of the mask

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	"source electrode",	mask", supra.	defining the edges of	film 20 shown in FIG.
	"drain electrode," and	•	the selectively	2c are selectively
	"at least a part of the		removed region.	removed with said
	mask", namely, the			[drain and source]
	source and drain			electrode members 15,
	electrodes serve as at			16 serving at least as a
	least part of the			part of the mask to
	pattern placed above a			form drain electrode 5
	surface from which			and source electrode
	material is to be			6." '737 Patent, col. 2
	selectively removed,			lines 60-66.
	where the pattern is			
	made up of material	-		See also '737 Patent,
	that is resistive to the			Figs. 1d, 2d, 3c; col. 4
	removal technique			lines 2-6.
	relative to material to			
	be removed.			Extrinsic Evidence:
				U.S. Patent No.
				5,905,274 to Ahn et
		,		al., Figs. 1E, 4E; col. 2
-		•		lines 32-39; col. 6
				lines 55-61. Exh. 13.
				II S Patent No
				C.D. I atom Ivo.

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Defendants' Support	6,025,605 to Lyu, Figs. 2D, 3I; Col. 1 lines 60-64; col. 2 lines 49-52; col. 4 lines 8-12. Exh. 14.	Intrinsic Evidence: '737 patent, Figs. 2a- 2e, 3a-3d; col. 1 lines 14-17, 21-31; col. 2 lines 8-35, 60-66; col. 3 lines 36-57 Extrinsic Evidence: "Form" is defined as "to give form or shape to; to give a particular shape to; to serve to make up or constitute." 1981
Defendants' Construction		Giving form or shape to above and supported by or in contact with.
LPL's Support		Intrinsic Evidence: '737 patent at col. 1, lines 14-17; col. 2, lines 8-17; Figs. 1a, 2a, 3a.
LPL's Construction		Providing above and supported by or in contact with.
Claim Term		"forming on"

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EXHIBIT E

EXHIBIT E

1-LA/750424.1

CLAIM TERMS	AGREED CONSTRUCTION
"substrate"	The material (such as glass) upon which a transistor or
	integrated circuit is fabricated to provide mechanical
	support.
"overlying"	Above.
"contact hole"	An opening formed in one or more insulative layers to
	expose a portion of a conductive layer for purposes of
	forming an electrical connection.
"via hole"	An opening formed in one or more insulative layers to
	expose a portion of a conductive layer for purposes of
	forming an electrical connection between two metallization
	patterns.
"liquid crystal display	A type of display that generates an image by directing light
device"	through an array of liquid crystal pixels, where the amount
	of light effused by each pixel is controlled via an electric
	field varying the orientation of the liquid crystal molecules
	contained within the pixel.
"material suitable for forming	A transparent, electrically conductive material that can be
a pixel electrode"	deposited and patterned, such as indium tin oxide (ITO).
"pixel electrode	A pattern of transparent electrically conductive material that
1	stores charge to drive the liquid crystal material within an
	individual element of the liquid crystal display device.
"patterning"	The removal of selected portions of a surface using etching
	techniques in order to produce a pattern in the remaining
	material.

CLAIM TERMS	AGREED CONSTRUCTION
"insulative layer" and	A thickness of non-conductive material (such as SiNx) that
"insulating film"	has high electrical resistance.
"indium tin oxide layer"	A thickness of indium tin oxide (ITO).
"semiconductor layer"	A thickness of a semiconductor material, such as amorphous
	silicon.
"impurity-doped	A thickness of semiconductor material, such as amorphous
semiconductor layer"	silicon, to which impurities (such as phosphorous atoms)
	have been added to enhance electrical conductivity.
"passivation layer"	A thickness of insulative material that provides protection
	such as electrical stability and chemical isolation.
"transparent conductive	A thickness of transparent electrically conductive material.
layer"	
conductive layer	A thickness of electrically conductive material.
one of a plurality of terminals	One of the terminals (i.e., source, drain, or gate) of a thin
of a thin film transistor	film transistor.

EXHIBIT F

EXHIBIT F

1-LA/750423.1

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F

U.S. Patent No. 5,825,449

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Defendant's Support	Intrinsic Evidence:	"As shown in FIG. 2c,	a conductive layer for	forming source	electrode 7 and drain	electrode 8 is deposited	on the substrate by	patterning a sputtered	layer of conductive	material." '449 Patent,	col. 3 lines 63-66	(emphasis added).		"As shown in FIG. 2d,	a passivation layer 9,	e.g., a nitride film, is	deposited on the entire	surface of the substrate	by a CVD process."	'449 Patent, col. 4 lines	6-8 (emphasis added).		"As shown in FIG. 2e,	an indium tin oxide
Defendants' Construction	Above and supported	by or in contact with.																						
LPL's Support	Intrinsic Evidence:	'449 patent claims 1,	6, 8, 10, 11 (compare	use of "on" with use	of "overlying").		" forming a first	conductive layer	pattern on a substrate.	. forming a second	insulative laver	overlying said	substrate" Claim	8 (emphasis added).	•	" a source electrode	and a drain electrode	on said semiconductor	laver a passivation	laver overlying said	source pad"	Claim 10 (emphasis	added).	
LPL's Construction	Touching a top or side	of.		LPL believes this term	has the same meaning	as "formed on" and	"disposed on", infra.	•																
Claim Term	OU													·	·									

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

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Defendant's Support		(ITO) layer is next	deposited on the	substrate by sputtering	or a CVD process"	'449 Patent, col. 4 lines	16-19 (emphasis	added).		See also '449 Patent,	Figs. 1-3, 5; Col. 1	lines 15-19, 34-64; col.	2 lines 5-13, 37-41, 56-	67; col. 3 lines 44-66;	col. 4 lines 39-41, 65-	68; col. 5 lines 1-17;	Claims 1, 2, 6, 8, 10,	1.		Extrinsic Evidence:	"On" is defined as "1.a.	Used to indicate	position above and	supported by or in	contact with: The vase
Defendants'	Construction																								
LPL's Support		" patterning said	second conductive	layer to form source	electrode and a drain	electrode on said	active layer; forming a	passivation film	overlying said	substrate including	said source pad"	Claim 11 (emphasis	added).		"An amorphous	silicon active layer 4	is formed on a portion	of gate insulating film	3 overlying gate 2."	'449 patent at 1:42-44	(emphasis added.)		See also '449 patent at	1:31-48, 56-64, 2:37-	46, 3:44-62, 4:19-23,
LPL's Construction													•												
Claim Term							_																		

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						'																		
Defendant's Support	is on the table. b. Used	to indicate contact with	or extent over (a	surface) regardless of	position: A picture on	the wall."	The American Heritage	College Dictionary 953	(3d ed. 1997), Exh. 8.		"On" is defined as "1.	- Used to indicate: a.	Position above and in	contact with <the td="" vase<=""><td>is on the bureau$>$ b.</td><td>Contact with a surface,</td><td>regardless of position</td><td><a on="" painting="" td="" the<=""><td>wall>." Webster's II</td><td>New College</td><td>Dictionary 764 (1995)</td><td>("1995 Webster's"),</td><td>Exh. 6.</td><td></td></td></the>	is on the bureau $>$ b.	Contact with a surface,	regardless of position	<a on="" painting="" td="" the<=""><td>wall>." Webster's II</td><td>New College</td><td>Dictionary 764 (1995)</td><td>("1995 Webster's"),</td><td>Exh. 6.</td><td></td>	wall>." Webster's II	New College	Dictionary 764 (1995)	("1995 Webster's"),	Exh. 6.	
Defendants' Construction																					ŗ			
LPL's Support	4:39-41, 4:65-5:7;	Figs. 1a-f, 2a-e, 3;	Claims 1, 2, 6, 8, 10,	11; '449 patent	prosecution history,	including Office	Action of 8/1/97 at p.	2.		Extrinsic Evidence:	1997 American	Heritage Dictionary at	953 (defining "on" as	"[u]sed to indicate	contact with or extent	over (a surface)	regardless of	position") (LPL Exh.	5); id. at 974 (defining	"overlie" as "to lie	over or on"); id. at 972	(defining "over" as	"[i]n or at a position	above or higher than:
LPL's Construction																								
Claim Term										•											•			

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		a sion over the door").		"Overlie" is defined as
		,		"to lie over or on" or
				"to lie over or upon."
				The American Heritage
				College Dictionary 974
				(3d ed. 1997), Exh. 8;
				1995 Webster's 783,
				Exh. 6.
formed on	Touching a top or side	See support for claim	Formed above and	See support for claim
		term "on" supra.	supported by or in	term "on" above.
			contact with.	
	LPL believes this term			
	has the same meaning			
	as "on", supra, and			
	"disposed on", infra.			
disposed on	Touching a top or side	See support for the	Arrange above and	See support for claim
4	of.	term "on", supra.	supported by or in	term "on" above.
			contact with.	£
	LPL believes this term			Extrinsic Evidence:
	has the same meaning			"Dispose" is defined as
	as "on" and "formed			"to arrange in a
	on", contract			particular order". 1995
	OII, supra.		_	Webster's 329, Exh. 6.
**	TT	Intrincio Biridence.	A contact hole is made	Intrinsic Evidence:
contact hole 18	I he contact hole is	HILLINSIC EVIDENCE.	A Contact field is a second	

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			/		
Defendant's Support	'449 Patent, Figs. 1c-1f, 2d-2e, 3, 5 (showing contact holes made in one side and out the opposite side).	See also '449 Patent, col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38.	Extrinsic Evidence: "Through" is defined as "in one side and out the opposite or another side". 1995 Webster's 1150 (1995), Exh. 6.	See also agreed construction for "contact hole."	Intrinsic Evidence: '449 Patent, Figs. 1c-
Defendants' Construction	in one side and out the opposite side.				Made in one side and out the opposite side.
LPL's Support	Figs. 1b-1f, 2b-2e, 3-5; 1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47.	("indium tin oxide layer extends through said first and second contact holes") with Figure 5 (showing	indium in oxide layer 6D entering one side of holes in insulative films 3 and 9 but not exiting out the opposite side).		See definition of "contact hole is
LPL's Construction	formed in the layer.				See definition of "contact hole is
Claim Term	provided through layer				provided through

		<u> </u>			
Defendant's Support	1f, 2d-2e, 3, 5; Col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38.	Extrinsic Evidence: "Through" is defined as "in one side and out	the opposite or another side". Webster's II New College Extrinsic	Evidence 1150 (1995) ("1995 Webster's"), Exh. 6.	See also agreed construction for "contact hole."
Defendants' Construction					
LPL's Support	provided through layer", supra.				,
LPL's Construction	provided through layer", supra.				
Claim Term					

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

LPL	LPL's Construction LPL's Support	pport	Defendants' Construction	Defendant's Support
A three terminal Int	Intrinsic Evidence:	ence:	A semiconductor	Intrinsic Evidence:
<u>.</u>	449 patent at 1:22-33;	1:22-33;	device in which the	449 Patent, Figs. 1-5;
in which the current Fig	Figs. 1-6.		current flow between	Col. 1 imes 13-55.
	449 natent	•	drain electrode is	Extrinsic Evidence:
is	prosecution history,	istory,	controlled by an	"Thin film technology"
	including Amendment	endment	electric field that	for circuits and systems
/ au	of 11/17/97 at p. 5	tp. 5	penetrates the	is defined as "a
electric field that	("The terminals of a	als of a	semiconductor; this	technology in which a
	thin film transistor	sistor	field is introduced by a	thin film (a few
r; this	correspond to the gate,	the gate,	voltage applied at the	hundred to a few
<u>~</u>	source, and drain.")	rain.")	gate electrode, which is	thousand angstroms in
	(LPL Exh. 3). See	. See	separated from the	thickness) is applied by
the	also Amendment of	nent of	semiconductor by an	vacuum deposition to
	11/17/97 at pp. 2-7.	5. 2-7.	insulating layer. The	an insulating
ı the			thin-film transistor is	substrate". 1984 IEEE
<u> </u>	Extrinsic Evidence:	dence:	formed using thin-film	939, Exh. 2.
insulating layer. The 19	1998 Penguin 569	695	techniques on an	
	"thin-film transistor	insistor	insulating substrate.	Paul K. Weimer, The
=	(TFT) A MOSFET	SFET		TFT – A New Thin-
	that is fabricated using	ted using		Film Transistor in 49
ite	thin-film techniques	niques		Proceedings of the IRE
rather than in a single or	on an insulating	gu		1462-64 (1962). Exh.
crystal silicon wafer.	substrate rather than	er than		7.

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Defendant's Support																								
Defendants' Construction																								
LPL's Support	on a semiconductor	chip.") (LPL Exh. 6);	id. at 205-207 ("field-	effect transistor (FET)	It is a three	terminal	semiconductor device	in which the current	flow through one pair	of terminals, the	source and the drain,	is controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	the voltage applied at	the third terminal, the	gate"); id. at 70	$("chip \dots A small")$	piece of single crystal	of semiconductor	material containing
LPL's Construction																				•	_			
Claim Term																								

Defendant's Support		Intrinsic Evidence: '449 Patent, Figs. 2d- 2e, 3, 5; Col. 4 lines 6- 26, 47-64; col. 5 lines 8-22, 33-38.
Defendants' Defendants' Construction		Having a selected 44 portion of the substance of the first 2e, and second insulating 26, layers removed using 8-2 an etching technique.
LPL's Support	either a single component or device or an integrated circuit.").	Intrinsic Evidence: '449 patent at 1:47-55, 2:8-10, 31-36. 50-51, 3:59-61, 3:67-4:1, 4:8-19, 35-39, 47-50, 5:1-15, 40-47; Figs. 1b-f, 2b-e, 3; Claims 8, 9, 11.
LPL's Construction		Removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired
Claim Term		selectively etching

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						<i>!</i>																		
Defendant's Support	for applying a voltage	in order to drive the	active layer in the	completed TFT	device." '449 Patent,	col. 3 lines 44-49.		See also '449 Patent,	Figs. 1-3, 5; col. 4,	lines 50-53.		Extrinsic Evidence:	"Gate" is defined as a	structural element of a	TFT that "controls the	current between source	and drain by a voltage	applied to its terminal".	1984 IEEE 384, Exh.	2.		"Gate" is defined as	"[a]n electrode or	electrodes in a field-
Defendants' Construction																								
LPL's Support	FIG. 2a, a conductive	layer is formed on a	transparent glass	substrate I and	patterned to form a	gate electrode 2, a	storage capacitor	electrode 2D, and a	gate pad 2C, all of the	same material. The	gate electrode is used	for applying a voltage	in order to drive the	active layer in the	completed TFT	device." '449 Patent,	3:44-49.		See also '449 patent at	1:22-38, 56-60, 2:37-	44, 2:56-61, 3:44-49,	4:47-53; 5:29-38;	Figs. 1a-f, 2a-e, 3-6;	Claims 10-11.
LPL's Construction															•									"
Claim Term																								

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Defendant's Support	effect transistor." The Penguin Dictionary of Electronics, 237 (2nd. ed. 1988) ("1988 Penguin"), Exh. 10.	Intrinsic Evidence: "Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively." '449 Patent, col. 1 lines 27- 30. "Gate pad 2B is used for receiving a voltage to drive and active
Defendants' Construction		A portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array that is necessary to communicate information from an external driving circuit to a gate electrode.
LPL's Support	·	"[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1.
LPL's Construction		A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a gate driving circuit.
Claim Term		gate pad

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Defendant's Support	layer in the completed	TFT device." '449	Patent, col. 1 lines 34-	38.		"Since a pad wiring	layer is necessary in	order to communicate	information from an	external driving circuit	to the gate and source,	a gate insulating film 3	is selectively etched to	expose source pad 2A	and gate pad 2B (see	FIG. 1c)." '449 Patent,	col. 1 lines 52-55.		"Then, a predetermined	portion of passivation	layer 9 and gate	insulating film 3 are	selectively etched	thereby exposing a
Defendants' Construction								·																
LPL's Support	material, as in the	conventional method,	and is formed at the	same time as gate 2,	storage capacitor	electrode 2D and gate	pad 2B." '449 patent	at 4:51-53.		See also '449 patent at	1:22-38, 1:52-60, 2:8-	10, 2:19-26, 3:44-49,	4:6-14, 4:21-27, 4:35-	41, 4:47-53, 4:65-5:1,	5:19-23; Figs. 1a-f, 3,	6; Claims 10-11.		Extrinsic Evidence:	1998 Penguin at 47	(defining "bonding	pads" as "[m]etal pads	arranged on a	semiconductor chip	(usually around the
LPL's Construction																								
Claim Term									,															

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Defendant's Support	predetermined region of gate pad 2C. For external electrical	connections It is necessary to exposed	pads 7A and 2C [sic]." '449 Patent, col. 4 lines	See also '449 Patent	Figs. 1-3, 5; Claims 10-11.	Extrinsic Evidence:	"Gate" is defined as the	structural element of a	thin film transistor that	between source and	drain by a voltage	applied to its terminal."	1984 IEEE 384, Exh.	.5
Defendants' Construction				- -	,									
LPL's Support	edge) to which wires may be bonded so that electrical connection	can be made to the component(s) or	circuit(s) on the chip.") (LPL Exh. 6).											
LPL's Construction														
Claim Term														

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
				European Patent No.
				530834 to Matsuda,
				Figs. 1 and 3, Col. 4
				lines 14-25, Exh. 9.
. 				See also support cited
				by LPL for the term
				"gad pad."
source pad	A portion of patterned,	Intrinsic Evidence:	A portion of patterned	Intrinsic Evidence:
	electrically conductive	"[A] conductive layer	electrically conductive	"Gate Pads 630 and
	material that is	is formed on a	material that is	Data Pads 640 are
	provided near the	transparent glass	provided near the	connected to the gate
	periphery of the thin	substrate 1 and	periphery of the thin	lines and data lines to
	film transistor array to	patterned to form gate	film transistor array	receive datas from gate
	receive data from a	2, a storage capacitor	that is necessary to	driver and data driver
	data driving circuit.	electrode 2D, a source	communicate	respectively." '449
		pad 2A and a gate pad	information from an	Patent, Col. 1 lines 27-
		2B. '449 patent at	external driving circuit	30.
		4:65-5:1.	to a source electrode.	
				"Since a pad wiring
		"[S]ource pad 2A is		layer is necessary in
		composed of gate		order to communicate
		material, as in the		information from an
		conventional method,		external driving circuit

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		and is formed at the		to the gate and source,
		same time as gate 2,		a gate insulating film 3
		storage capacitor		is selectively etched to
		electrode 2D and gate		expose source pad 2A
		pad 2B." '449 patent		and gate pad 2B (see
		at 4:51-53.		FIG. 1c)." '449 Patent,
_				col. 1 lines 52-55.
		See also '449 patent at		
		1:8-12, 1:22-38, 1:52-		"Then, a predetermined
	-	64, 2:8-10, 2:17-22,		portion of passivation
		3:66-4:5, 4:6-14, 4:24-		layer 9 and gate
		27, 4:35-61, 4:65-5:1,		insulating film 3 are
		5:19-23, 5:48-51;		selectively etched
		Figs. 1a-f, 2d-e, 3, 6;		thereby exposing a
		Claims 10-11.		predetermined region
				of source pad 7A
		Extrinsic Evidence:		For external electrical
		1998 Penguin at 47		connections It is
		(defining "bonding		necessary to exposed
		pads" as "[m]etal pads		pads 7A and 2C." '449
		arranged on a		Patent, col. 4 lines 8-
		semiconductor chip		15.
		(usually around the		
		edge) to which wires		See also '449 Patent,

																	 		-		
Defendant's Support	Figs. 1-3, 5; Claims 10-11.		Extrinsic Evidence:	"Source" is defined as	the structural element	of a thin film transistor	that "contains the	terminal from which	charge carries flow into	channel toward the	drain. It has the	potential which is less	attractive than the drain	for the carriers in the	channel". 1984 IEEE	855, Exh. 2.	European Patent No.	530834 to Matsuda,	Figs. 1 and 3, Col. 4	lines 14-25, Exh 9.	See also support cited
Defendants' Construction									·								•				
LPL's Support	may be bonded so that	can be made to the	component(s) or	circuit(s) on the	chip.") (LPL Exh. 6).																-
LPL's Construction						-															
Claim Term																					

Defendant's Support	by LPL for the term "source pad."	Intrinsic Evidence:	'449 Patent, Figs. 1b-	1f, 2b-2e, 3, 5; Col. 1	lines 39-41; col. 3 lines	50-52; col. 5 lines 1-4		Extrinsic Evidence:	"Gate" is defined as the
Defendants' Construction		A thickness of non-	conductive material	(such as SiNx) that has	high electrical	resistance and insulates	the gate electrode from	the semiconductor.	
LPL's Support		Intrinsic Evidence:	'449 patent at 1:40:44,	1:52-55, 2:11-13,	2:19-26, 2:34-36,	2:40-44, 3:50-53, 4:1-	15, 4:35-39, 4:47-50,	4:65-5:4, 5:12-15,	5:19-23. 5:40-46:
LPL's Construction		A thickness of	non-conductive	material (such as	SiNx) that has high	electrical resistance	and insulates the	transistor gate from	the semiconductor.
Claim Term		gate insulating	film						

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JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F U.S. Patent No. 5,825,449

Defendant's Support	structural element of a	"controls the current	between source and	drain by a voltage	applied to its terminal."	1984 IEEE 384, Exh.	2.		"Insulating material" is	defined as "a substance	or body, the	conductivity or which	is zero or, in practice,	very small." 1984	IEEE 447, Exh. 2.		'Film" is defined as "a	thin skin or	membranous coating",	"a thin coating". 1995	Webster's 419, Exh. 6.	"Layer" is defined as a
Defendants' Construction																						
LPL's Support	Figs. 1b-f, 2b-e, 3, 5;	Claim 10.	Extrinsic Evidence:	1998 Penguin at 209	(defining "film" as a	"coating with a	minimal thickness	dimension.") (LPL	Exh. 6).		1997 American	Heritage Dictionary at	770 (defining "layer"	as a "thickness of	material covering a	surface or forming an	overlying part or	segment.") (LPL Exh.	5).			
LPL's Construction													,									
Claim Term																						

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

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Defendant's Support	"thickness of material	covering a surface or	forming an overlying	part or segment."	1997 American	Heritage Dictionary	770, LPL Exh. 5.	Intrinsic Evidence:	"As shown in FIG. 1e,	the TFT is formed on	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In the	completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring
Defendants' Construction								A conductive element	of a single thin-film	transistor formed over	the source region from	which charge carriers	flow into the channel	toward the drain. The	source electrode is	distinct from the	source/data line and the	source/data pad	associated with the	source electrode.				
LPL's Support								Intrinsic Evidence:	"As shown in FIG. 1e,	the TFT is formed on	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively. Source	electrode 7 is	connected to source	pad 2A, and drain	electrode 8 is contact	with impurity-doped
LPL's Construction								A patterned,	electrically conductive	material formed over	the source region.	Current flows through	the channel between	the source electrode	and drain electrode	under control of the	gate electrode.							
Claim Term								source electrode															2 W	

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Defendant's Support	layer and drain	electrode 8, to pixel	electrode 6." '449	Patent, col. 1 line 61 –	col. 2 line 2.		"As shown in FIG. 2c,	a conductive layer for	forming source	electrode 7 and drain	electrode 8 is deposited	on the substrate by	patterning a sputtered	layer of conductive	material. Using the	source and drain	electrodes as masks,	portions of the	impurity-doped	semiconductor layer 5	are exposed and then	etched. Source	electrode 7 thus forms	part of a transistor
Defendants' Construction																								
LPL's Support	semiconductor layer 5	and pixel electrode 6.	In the completed	device structure,	source electrode 7	conducts a data signal,	received from a data	wiring layer and drain	electrode 8, to pixel	electrode 6. The signal	is stored in the form of	charge on pixel	electrode 6, thereby	driving the liquid	crystal." '449 patent	at 1:61-2:4.		"[P]ortions of the	impurity-doped	semiconductor layer 5	are exposed and then	etched. Source	electrode 7 thus forms	part of a transistor
LPL's Construction																								
Claim Term																								

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

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Defendant's Support	region and serves as	source pad 7A above	the gate insulating film	so that the same	conductive layer	constitutes part of the	source wiring and the	source electrode of the	TFT." '449 Patent,	col. 3 line $63 - \text{col. 4}$	line 5.		"Then, a conductive	layer is formed on the	substrate and etched in	accordance with a	predetermined pattern,	thereby forming a	source electrode 7 and	a drain electrode 8."	'449 Patent, col. 5 lines	6-8.		See also '449 Patent,
Defendants' Construction																								
LPL's Support	region and serves as	source pad 7A above	the gate insulating	film so that the same	conductive layer	constitutes part of the	source wiring and the	source electrode of the	TFT." '449 patent at	3:67-4:5.		"[S]ince both the first	(45) and fourth (60)	contact holes are	formed over source	pad 2A (formed of the	same material as the	gate) and source	electrode 7,	respectively, the	source electrode 7 and	source pad 2A may be	connected to each	other in the same step
LPL's Construction													/									-		
Claim Term																		-						

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

Defendant's Support	Figs. 1e-1f, 2c-2e, 3, 5;	col. 1 lines 9-12; col. 2	lines 11-13.		Extrinsic Evidence:	"Source" is defined as	a device structure	which "contains the	terminal from which	charge carries flow into	the channel toward the	drain. It has the	potential which is less	attractive than the drain	for the carriers in the	channel." 1984 IEEE	855, Exh. 2.	,	"Source" is defined as	"[t]he electrode in a	field-effect transistor	that supplies charge	carriers (holes or	electrons) to the
Defendants' D Construction	Fig	col	line		EXI	os,		wh	teri	cha	the	dra	bot	attr	for	cha	855			[1],	fiel	tha	can	elec
LPL's Support	that the pixel electrode	is formed. Thus, after	patterning, a first	transparent conductive	layer 6C connects	source electrode 7	with source pad 2A,	and a second	transparent conductive	layer 6 (i.e., the pixel	electrode) is	connected to drain	electrode 8." '449	patent at 4:56-64.		See also '449 patent	1:8-12, 1:22-30, 1:61-	2:4, 2:11-27, 2:37-	3:15, 3:63-4:5, 4:47-	64, 5:6-15, 5:29-39,	5:48-54; Figs. 1e-f,	2c-e, 3-6, Claims 10,	11.	
LPL's Construction																								
Claim Term																								

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

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Defendant's Support	interelectrode space." 1998 Penguin 532, Exh. 10.	Intrinsic Evidence: "As shown in FIG. 1e,	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In the	completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring	layer and drain	electrode 8, to pixel	electrode 6." '449
Defendants' Construction		A conductive element of a single thin-film	the drain region into	which charge carriers	flow from the source	into the channel.													
LPL's Support		Intrinsic Evidence: "As shown in FIG. 1e,	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In	the completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring	layer and drain	electrode 8, to pixel	electrode 6. The
LPL's Construction		A patterned, electrically conductive	material formed over the drain region.	Current flows through	the channel between	the source electrode	and drain electrode	under control of the	gate electrode.										
Claim Term		drain electrode																	

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

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Carpoort	Defendant's Support	line 61 –		,	uctive	layer is formed on the	substrate and etched in	ith a	predetermined pattern,	ng a	source electrode 7 and	de 8."	'449 Patent, col. 5 lines		Patent.	Figs. 1e-1f. 2c-2e, 3, 5.		lence:	"Drain" is defined as a	device structure which	"contains the terminal	arge	carriers flow from the	source into the channel.
1000	เเนสเน ร	Patent, col. 1 line 61	line 2.		"Then, a conductive	s forme	ate and	accordance with a	erminec	thereby forming a	electro	a drain electrode 8."	atent, c		See also '449 Patent.	e-1f. 2	•	Extrinsic Evidence:	ı" is del	structu	ins the	into which charge	s flow	into th
25.07	Dele	Patent	col. 2 line 2.		Then .	layer i	substr	accord	predet	thereb	source	a drair	,449 F	6-8.	See al	Figs.	5	Extrin	"Drain	device	"conta	into w	carrie	source
D. C. 1-1-2	Defendants Construction																					-		
	LPL's Support	signal is stored in the	form of charge on	pixel electrode 6,	thereby driving the	liquid crystal." '449	patent at 1:61-2:4. See	also '449 patent at	1:8-12, 1:22-30, 1:61-	2:4, 2:11-27, 2:37-	3:15, 3:63-4:5, 4:17-	27, 4:47-64, 5:6-22;	Figs. 1e-f, 2c-e, 3-6,	Claims 10, 11.										
	LPL's Construction																						•	
	Claim Term														- Contract									

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F U.S. Patent No. 5,825,449

LPL's Construction
Intrinsic Evidence:
449 patent at 1:34-51
1:61-2:4, 2:11-27,
3:44-62, 4:65-5:5
5:39-47; Figs. 1b-f,
20-e, 3, 5; Claim 11
Extrinsic Evidence:
1997 American

JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F U.S. Patent No. 5,825,449

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendant's Support
			Construction	
	electric field	Heritage Dictionary at		covering a surface or
	introduced by the gate	770 (defining "layer"		forming an overlying
	electrode.	as a "thickness of		part or segment." 1997
		material covering a		American Heritage
		surface or forming an		Dictionary 770, LPL
		overlying part or		Exh. 5.
		segment.") (LPL Exh.		
		5).		
common hole	A shared hole.	Intrinsic Evidence:	A single hole.	Intrinsic Evidence:
		'449 patent at 4:47-64;		'449 Patent, Figs. 3, 5;
		5:8-22, 33-38; Figs. 3,		Col. 4 lines 47-64; col.
		5; claim 4.		5 lines 8-22, 33-38.
		Extrinsic Evidence:		Extrinsic Evidence:
		1997 American		"Common" is defined
		Heritage Dictionary at		as "belonging to,
		281 (defining		shared by, or applying
		"common" as		equally" 1995
	,	"[b]elonging equally		Webster's 226. Exh 2.
		to or shared equally by		
		two or more; joint.")		
		(LPL Exh. 5).		
aligned	Placed in line with.	Intrinsic Evidence:	Substantially co-axial	Intrinsic Evidence:
		'449 patent at 4:47-64;	or concentric.	'449 Patent, Figs. 3, 5;

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

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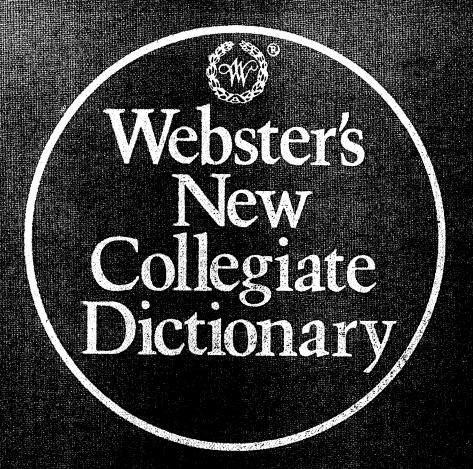
Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		5:8-22, 33-38; Figs. 3, 5; claim 5.		Col. 4 lines 47-64; col. 5 lines 8-22, 33-38.
		Extrinsic Evidence: 1997 American		Extrinsic Evidence: "Align" is defined as
		Heritage Dictionary at 34 (defining "align"		"to place in a line." 1995 Webster's 28.
		as [1]0 an ange in a line) (LPL Exh. 5).		
said second	The second insulating	Intrinsic Evidence:	The second deposited	Intrinsic Evidence:
insulating layer	layer includes "a	'449 patent at 2:37-55;	layer of insulating	'449 Patent, Figs. 3, 5;
having a second	second contact hole"	3:2-14; 4:47-64; 5:8-	material has a second	Col. 4 lines 47-64; col.
contact hole	that exposes a portion	22, 33-38; Figs. 3, 5;	contact hole through it	5 lines 8-22, 33-38.
exposing a	of the second	claims 1, 2, 5, 6, 8, 10,	which: (a) uncovers a	
predetermined	conductive layer. The	and 11.	selected portion of the	
portion of said	second insulating		second deposited	
second	layer also includes		conductive layer and	
conductive layer	"said first contact hole		(b) uncovers the region	
and said first	region", i.e., it		in which the first	•
contact hole	includes part of the		contact hole is located.	
region	first contact hole		The first and second	
	which exposes the		contact holes must	
	predetermined portion	•	overlap.	

Document 389-9

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

		γ							· · ·						
Defendant's Support		Intrinsic Evidence: "The TFT of the	present invention having electrical	contacts or wiring	structures including	gate pad 2C, layer 6B	and layer 6A, source	pad 7A is thus	completed." '449	Patent, Col. 4 lines 24-	26; Figs. 1-5.	See also '449 Patent,	Col. 1 lines 52-55; col.	2 lines 1, 16-18; col. 4	lines 1-5.
Defendants' Construction		A structure providing an electrically	conductive path that connects at least two	terminals.											
LPL's Support		Intrinsic Evidence: '449 patent at 4:24-27.	Extrinsic Evidence:	1997 American	Heritage Dictionary at	1547-1548 (defining	"wire" as "resembling	a wire, as in	slendemess") (LPL	Exh. 5).					
LPL's Construction	of the first conductive layer.	A slender structure electrically connecting	at least two points.												
Claim Term		wiring structure													

EXHIBIT L-4(c)



a Merriam-Webster

New Collegiate Dictionary

A Merriam-Webster®

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Library of Congress Cataloging in Publication Data Main entry under title:

Webster's new collegiate dictionary.

Editions for 1898-1948 have title: Webster's collegiate dictionary. Includes index. 1. English language—Dictionaries.

PE1628.W4M4 1980 423 79-24073 ISBN 0-87779-398-0

ISBN 0-87779-399-9 (indexed)

ISBN 0-87779-400-6 (deluxe)

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fore-time \fo(3)r_tim, 'fo(3)r_\ n: former or past time: the time before the present 'fore-to-ken \fo(3)r_\tō-kən, 'fo(3)r_\ n: a premonitory sign 'fore-to-ken \fo(3)r_\tō-kən, for-\ vt fore-to-kened; fore-to-ken-ing \-'tōk-(2-)nin\: to indicate or warn of in advance fore-top \fo(3)r_\tāp, 'fo(3)r_\ in sense 2 often 'fōrt-3p or 'fort-\ n 1: hair on the forepart of the head; esp: the forelock of a horse 2: the platform at the head of a ship's foremast fore-top-gal-lant \for-\tap-gal-ant, 'for-\ fort-3p_\ gal-\, 'fort-\ adj: being the part next above the fore-topmast fore-top-man \for-\tap-man, 'for-\ fort-3p_\, 'fort-\ n: a sailor on duty on the foremast and above fore-top-mast \for-\tap-man, 'for-\ fort-3p_\ mast, 'for-\ n: a mast next above the foremast \for-\tap-man, 'for-\ fort-3p_\ mast, 'for-\ n: the sail above fore-top-sail \for-\tap-\tap-\tap-\tap-\, 'fort-\ p-\, 'fort-\ n: the sail above

fore-top-sail \for-,tap-sal, for-; fort-ap-, fort-\ n: the sail above the foresail

'for-ever \fo-'rev-or, fo-\ adv 1: for a limitless time \(\warmanneq\) to live \sim \ 2: at all times \(\sin\) is \sim jingling the change in his pocket\(\sin\) 2forever n: an unspecified length of time \(\sin\) it took her \sim to find the

for-ever-more \-,rev-ə(r)-'mō(ə)r, -'mo(ə)r\ adv: FOREVER for-ev-er-ness \-'rev-ər-nəs\ n: ETERNITY for-warn \for-'wo(ə)rn, for-\ vt: to warn in advance syn see

forewarn (10f-w0(3)ff), 10f-\ vi : 10 warn in advance syn see WARN

fore wing n: either of the anterior wings of a 4-winged insect
foreworn an \fo(3)r-\wim wim-3n, \fo(3)r-\ n: FORELADY
foreword \for-\(\frac{1}{10}\), \for-\(\fra

where metal is neated and wrought: SMITHY 2: a workshop where wrought iron is produced or where iron is made malleable forge by forged; forging w 1 a: to form (as metal) by heating and hammering b: to form (metal) by a mechanical or hydraulic press with or without heat 2: to form or bring into being esp. by an expenditure of effort (made every effort to ~ party unity) 3: to make or imitate falsely esp. with intent to defraud: COUNTERFEIT ~ wi 1: to work at a forge 2: to commit forgery — forgeability \(\) \(\text{for-jo-bil-ot-\vec{e}}, \(\text{for-\)\(\) \(n \) — forge-able \(\text{for-jo-bol}, \(\text{for-\)\(\) \

adj

3forge vi forged; forg-ing [origin unknown] 1: to move forward slowly and steadily (the great ship forged ahead through the waves) 2: to move with a sudden increase of speed and power (the horse forged into the lead in the homestretch) forger \(\forger \forger \for

forger \Tof-jər, Tor-\ n 1 a: one that taisines; specij: a creator of false tales b: a person guilty of forgery 2: one that forges metals forge-ry \text{\forj-\n.pl.-er-les} 1 \ archaic: Invention 2: an act of forging; esp: the crime of falsely and fraudulently making or altering a document (as a check) 3: something forged for-get \text{\for-\text{yet}}, \ for-\text{\text{yet}} \ \ begot \text{\cap-gatty}, \ gotten \text{\cap-gatty} \ gatty \ or \ got \ \ gatty \ gatty \ gatty \ gatty \ gatty \ gatty \ or \ got \ or \ gatty \ gatty \ or \ got \ or \ got \ or \ gatty \ or \ or \ got \ or \ gatty \ or \ got \ or \ gatty \ or \ or \ got \ or \ gatty \ or \ got \ or \ gatty \ or \ got \ or \ go

for-giv-ing adj: willing or able to forgive — for-giv-ing-ly \-'giv-ing-l\(\alpha\) adv — for-giv-ing-ness n
for-go or fore-go \(\for\) for-go, for-\(\for\) w-went\\-'went\\; -gone \-'gon also
\-'gan\\; -go-ing\\-'go-ing\-'go-ing\-'go'-ln\\\[ME\forgon\), fr. OE\forgan\ to pass
by, forgo, fr. for-\(\for\) gan to go] \(\for\) archaic: Forsake \(\for\): to abstain
from: RENOUNCE \(\sigma\) immediate gratification for the sake of future
gains\(\righta\) — for-goet-\(\for\)-go-\(\for\)-\(\for\) for-\\\\\ n\\ i a\) person or category of
persons that receives less attention than is merited
for-int\(\for\) fo(\(\for\))r\\\\\ n\\ [Mung]\) — see Money table
for-judge var of ForeIUDGE

**fork \(\for\) fo(\(\for\))r\\\\\\\ n\\ [ME\forke\, fr. OE\(\for\) ONF; OE\(\for\) forca \(\for\) ONF
forque, fr. L\(\for\) funcal \(\for\) is an implement with two or more prongs
used esp. for taking up (as in eating), pitching, or digging \(\for\): a
forked part, tool, or piece of equipment \(\for\) a: a idivision into
branches or the place where something divides into branches b
: CONFLUENCE \(\for\) a: one of the branches into which something
forks \(\for\): Atternative, CHOICE \(\for\): an attack by one chess piece
(as a knight) on two pieces simultaneously — fork-ful\-\full\\(\for\) ful\\(\for\) n

*fork vi 1: to divide into two or more branches \(\sigma\) where the road
\(\sigma\): 2 a: to use or work with a fork \(\for\) in the fingers\(\for\) 2: to raise, pitch, dig, or work with a fork \(\sigma\) natice (\sigma\) in the operation one end divided into two or more branches or points \(\sigma\) in the operation one end divided into two or more branches or points \(\sigma\) in the operation one end divided into two or more branches or points \(\sigma\) in the operation of the procked \(\for\) for-kad\(\for\) adj 1: resembling a fork esp. in having one end divided into two or more branches or points \(\sigma\) in the operation of the procked \(\for\) for-kad\(\for\) and forked for hosting and transporting heavy objects by means of s

transporting heavy objects by means of steel fingers inserted under

syn form, figure, shape, conformation, configuration shared

syn FORM. FIGURE, SHAPE, CONFORMATION, CONFIGURATION shared meaning element: outward appearance

2form vi 1: to give form or shape to: FASHION 2 a: to give a particular shape to: shape or mold into a certain state or after a particular model: ARRANGE (~ed the dough into various shapes) (a state ~ed along the lines of the Roman Republic) b: to arrange themselves in (the women ~ed a line) c: to model by instruction and discipline (a mind ~ed by classical education) 3: DEVELOP, ACQUIRE (~a habit) 4: to serve to make up or constitute: be a usu. essential or basic element of 5 a: to assume an inflection so as to produce (as a tense) (~s the past in -ed) b: to combine to make (a compound word) c: to make up: CONSTI

* kitten a abut ər further a back ā bake ä cot, cart ch chin e less ē easy g gift i trip aŭ out n sing o flow o flaw oi coin th thin j joke th this ii loot ù foot yü few y yet yù furious

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form- of forsythia

TUTE (~ a clause) 6: to arrange in order: draw up ~ vi 1: to become formed or shaped 2: to take form: come into existence: ARISE 3: to take on a definite form, shape, or arrangement syn see MAKE—form-abili-ity \for-ma-bil-ite\ n — form-able \form-bol\ adj — form on: to take up a formation next to form-or formo-comb form [formic]: formic acid \(formate \) form \(adj \) comb form [MF & L; MF -forme, fr. L -formis, fr. \(formal \) in the form or shape of: resembling \((oviform) \) for-mal \(\formal \) in the form or shape of: resembling \((oviform) \) for-mal \(\formal \) in the form or shape of: resembling \((oviform) \) for-mal \(\formal \) if or -mal \(\formal \) did \(1 \) a: belonging to or being the essential constitution or structure \((\sim \cause \) b: relating to, concerned with, or constituting the outward form of something as distinguished from its content \(2 \) a: following or according with established form, custom, or rule: \(Conventional form \) according with established form, \(custom, or rule : Conventional form \(a \sim contract \) 3 a: based on conventional forms and rules b: characterized by punctilious respect for form: METHODICAL \(very \) in all his dealings \(c : rigidly \) ceremonious: \(PRIM \) 4: having the appearance without the substance \((\sim Christians \) who go to church only at Easter \(> syn \) see CEREMONIAL \(snt \) informal — for-mal-ly \(-mo-le\) adv — for-mal-ness \(n \). MOLAB ?

le\ aav — Tor-mai-ness n

formal n: something (as a dance or a dress) formal in character

formal adj [formula + -al]: \(^3\)MOLAR 2

form-al-de-hyde \(^for-\)mal-de-hid, for-\(^n\) [ISV form- + aldehyde]

: a colorless pungent irritating gas CH₂O used chiefly as a disinfector of the compounds and the compounds and tant and preservative and in synthesizing other compounds and resins

for-ma-lin \for-ma-lan, -lēn\ n [fr. Formalin, a trademark]: a clear aqueous solution of formaldehyde containing a small amount of

methanol

for-mal-ism \for-ma-,liz-am\ n: the practice or the doctrine of strict adherence to prescribed or external forms (as in religion or art); also: an instance of this — for-mal-ist \-last\ n or adj — for-mal-istic \-for-ma-'lis-tik\ adj — for-mal-istical-ly \-ti-k(2-)le\

for-mal-i-ty \for-mal-st-\(\bar{e}\)\ n, pl-ties 1: the quality or state of being formal 2: compliance with formal or conventional rules: CEREMONY 3: an established form that is required or conventional

fromal-ize \for-mə-,līz\ vt -ized; -iz-ing 1: to give a certain or definite form to: SHAPE 2 a: to make formal b: to give formal status or approval to — for-mal-iz-able \-,lī-zə-bəl\ adj — for-mal-iza-tion \for-mə-lə-'zā-shən\ n — for-mal-iz-er \for-mə-,lī-zə-bəl\ za-shən\ n — for-mal-iz-er \for-mə-,lī-zə-bəl\ za-shən\ n — for-mal-iz-er \for-mə-,lī-zə-bəl\ za-shən\ za-s

status or approval to — for-maliz-able _li-za-bəl\ adj — for-mal-iza-tion _for-mə-lə-'zā-shən\ n — for-maliz-er _for-mə-lī-zər\ n

formal logic n: a system of logic (as Aristotelian logic or symbolic logic) that abstracts the forms of thought from its content to establish abstract criteria of consistency

for-mant _for-mənt, -mant\ n: a characteristic component of the quality of a speech sound; specif: any of several resonance bands held to determine the phonetic quality of a vowel

for-mat _fo(s)r-mat\ n [F or G; F, fr. G, fr. L formatus, pp. of formare to form fr. formal 1: the shape, size, and general makeup (as of something printed) 2: general plan of organization or arrangement (as of a television show)

for-mat _fo(s)r-māt\ et or-mat\ ting: to produce in a specified form or style \(formatted \) output of a computer \(for-mat\) \(for-mat\) \(for-mat\) \(for-mat\) \(n: a \) salt or ester of formic acid for-mat\(for-mat\) \(for-mat\) \(for-mat\) \(n: a \) salt or ester of formic acid for-mat\(for-mat\) \(for-mat\) \(for-mat\) \(n: a \) salt or ester of formic acid for-mat\(for-mat\) \(for-mat\) \(for-mat\) \(for-mat\) \(a: b) \) \(for-mat\) \(for-mat\)

in some prescribed manner or for a particular purpose — for-mation-al\-shnal, -shnal\-1\ adj | 1 a: giving or capable of giving form: CONSTRUCTIVE (a ~ influence) b: used in word formation or inflection 2: capable of alteration by growth and development; also: producing new cells and tissues 3: of, relating to, or characterized by formative effects or formation (~ years) — formative-ly adv — for-ma-tive-ness n

2formative n 1: the element in a word that serves to give the word appropriate form and is not part of the base 2: the minimal syntactically functioning element in a transformational grammar

form class n: a class of linguistic forms that can be used in the same position in a construction and that have one or more morphological or syntactical features in common

phological or syntactical features in common form critical adj: based on or applying form criticism n: a method of criticism for determining the sources and historicity of esp. biblical writings through analysis of the writings in terms of traditional literary forms (as love poems, parables, and sayings)—form critic n formed \formal adj: organized in a way characteristic of living matter (mitochondria are \sim bodies of the cell) (red blood cells are

~ elements of the blood)
for-mée \for-mã, for-\ adj [ME forme, fr. MF formé] of a heraldic
cross: having the arms narrow at the center and expanding toward

cross: having the arms narrow at the center and expanding toward the ends — see CROSS illustration

'for-mer \'for-mer \ adj [ME, fr. forme first, fr. OE forma — more at FOREMOST]

1 a: coming before in time b: of, relating to, or occurring in the past (~ correspondence)

2: preceding in place or arrangement: FOREGOING (~ part of the chapter)

3: first mentioned or in order of two things mentioned or understood (of these two evils the ~ is the lesser)

syn see PRECEDING

ant latter

'form-er \'for-mor n

1: one that forms

2 chiefly Brit: a member of a school form — usu. used in combination (sixth ~)

for-mer-ly \'for-mo(r)-le\ adv

1 obs: just before

2: at an earlier time: PREVIOUSLY

form-fit-time \'form-fit-in\) adi: conforming to the outline of the

form-fit-ting \form-fit-in\ adj: conforming to the outline of the body: fitting snugly $\langle a \sim \text{sweater} \rangle$

form-ful \form-fol\ adj: exhibiting or notable for form (as in a

sport)
form genus n: an artificial taxonomic category established for organisms (as imperfect fungi) of obscure true relationships for-mic \(\text{for-mic}\) \(\text{for-mic}\) \(\text{doj}\) \(\text{L formica}\) ant \(-\text{more at PISMIRE}\): derived

from formic acid

For.mi-Ra \for-\mi-Ra, for-\ trademark — used for any of various laminated plastic products used esp. for surface finish

formic acid n: a colorless pungent fuming vesicant liquid acid

CH₂O₂ found esp. in ants and in many plants and used chiefly in dyeing and finishing textiles

for-mi-cary \'for-ma-,ker-e\ n, pl -car-les [ML formicarium, fr. L

formicary \for-mo-ker-e\ n, pl-car-ies [ML formicarium, fr. L formica]: an ant nest
for-mida-ble \for-mod-o-bol also for-mid- or for-mid-\ adj [ME, fr. L formida-ble \for-mod-o-bol also for-mid- or apprehension (a \sigma property 2: having qualities that discourage approach or attack 3: tending to inspire awe or wonder — for-mida-ble-ty \for-mod-o-bol-nos; for-mid-, for-\ n — for-mida-ble-noss \for-mod-o-bol-nos; for-mid-, for-\ n — for-mida-bly \cdot ble adv
form-less \for-mod-o-bol-nos; for-mid-sol also also physical existence — form-less-ly adv — form-less-ness n
form letter n 1: a letter on a subject of frequent recurrence that can be sent to different people without essential change except in the address 2: a letter that is printed in many copies, has a very general salutation (as Dear Friend), and is sent to a usu. large number of people.

- see FORMformoformu-la \formy-la\ n, pl -las or -lae \-,l\ ,-,l\ [L, dim. of forma form]

1 a: a set form of words for use in a ceremony or ritual b: a conventionalized statement intended to express some fundamental truth or principle esp. as a basis for negotiation or action 2 a (1): RECIPE (2): PRESCRIPTION b: a milk mixture or sub-2 a (1): RECIPE (2): PRESCRIPTION b: a milk mixture or substitute for feeding an infant 3 a: a general fact, rule, or principle expressed in symbols b: a symbolic expression of the chemical composition or constitution of a substance c: a group of numerical symbols associated to express briefly a single concept d: a combination of signs in a logical calculus 4: a prescribed or set form or method (as of writing): an established rule or custom—often used derogatorily (television programs that were unimaginative ~ works)—for-mu-la-ic \for-my-la-ik\ adj — for-mu-la-ical-ly \-la-s-k(x-)le\ adv
2formula adj, of a racing car: conforming to prescribed specifications as to size, weight, and engine displacement and usu. having a long narrow body, open wheels, a single-seat open cockpit, and the engine in the rear

for-mu-la-ri-za-tion \for-myə-lə-rə-'zā-shən\ n: an act or a prod-

for-mu-la-ri-za-tion \for-my-la-ra-'zā-shən\ n: an act or a product of formularizing for-mu-la-rize\'for-my-la-j-riz\ n! -rized; -riz-ing: to state in or reduce to a formula: FORMULATE — for-mu-la-riz-er n for-mu-la-ry\'for-my-ler-\(\inp\) n. p! -lar-ies 1: a book or other collection of stated and prescribed forms (as oaths or prayers) 2: a prescribed form or model: FORMULA 3: a book containing a list of medicinal substances and formulas — formulary adj for-mu-late\'for-my-lāt\' n' -lat-ed; -lat-ing 1 a: to reduce to or express in a formula b: to put into a systematized statement or expression c: DEVISE (~ policy) 2 a: to develop a formula for the preparation of (as a soap or plastic) b: to prepare according to a formula— for-mu-la-tor\-lat-ar\n n: an act or the product of for-mu-lation\-for-my-lā-shən\n: an act or the product of for-mu-lating

formula weight n: MOLECULAR WEIGHT — used esp. of ionic com-

pounds
for-mu-liza-tion \for-my--\for-m

for-ni-cate \for-no-,kāt\ vb -cat-ed; -cat-ing [LL fornicatus, pp. of fornicare, fr. L fornic, fornix arch, vault, brothel] vi: to commit fornication ~ vt: to commit fornication with — for-ni-ca-tor

\\\ \kat-\(\)r\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\ for-ni-\(\)r\\\\

unmarried person accomplished with consent and not deemed adultery for-nix \"for-niks\ n, pl for-ni-ces \-n--i-sēz\ [NL, fr. L]: an anatomical arch or fold for-red-er also for-rard-er \"far-əd-ər\ adv [E dial., compar. of E forward] chiefly Brit: further ahead for-sake \for-'sāk, for-\ vi for-sook \-'sūk\; for-sak-en \-'sā-kən\; for-sak-ing [ME forsaken, fr. OE forsacan, fr. for- + sacan to dispute; akin to OE sacu action at law — more at SAKE] 1: to renounce (as something once cherished) without intent to recover or resume (\sigma a bad habit) 2: to quit or leave entirely: withdraw from (forsook the theater for politics) syn see ABANDON and return (to), revert (to) for-sooth \for-'sūth\ adv [ME for soth, fr. OE forsōth, fr. for + sōth sooth]: in truth: INDEED — often used to imply contempt or doubt

for-spent \for-'spent, for-\ adj, archaic: worn out: EXHAUSTED for-swear or fore-swear \for-'swa(ə)r, for-, -'swe(ə)r\ vb -swore \-'swo(a)r, -'swo(a)r\; -sworn \-'swo(a)rn\; -swear-ing vt 1 a: to reject or renounce under oath b: to renounce earnestly 2: to deny under oath 3: to make a liar of (oneself) under or as if under oath \(\lambda \) himself\(\rangle \) vi: to swear falsely \(syn \)

for-sworn or fore-sworn \-'swo(\(\))rn, -'swo(\(\))rn\ adj: guilty of perjury: marked by perjury for-syth-ia \for-'sith-\(\)-\(\)\ [NL, genus name, fr. William Forsyth \+\)1804 Brit botanist]: any of a genus (Forsythia) of ornamental

EXHIBIT L-5

Ex. L-5 LGD US PATENT No. 5,825,449

INDEX OF DISPUTED TERMS

CLAIM TERMS	PAGE
wiring structure	9
conductive layer	1
layer	9
formed on a first portion of said substrate	14
formed on	14
formed on a second portion of said substrate	14
formed on a first portion of said first insulative layer	14
insulative layer	9
formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer	14
overlying	9
contact hole	16
provided through	16
expose part of said layer	16
extends through	16
one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor	21
one of said first and second conductive layers	1
one	1
connected to	1
one of a plurality of terminals of a thin film transistor	21
a plurality of terminals of a thin film transistor	21

Ex. L-5 LGD US PATENT No. 5,825,449

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	PAGE
thin film transistor	21
liquid crystal display device	24
gate electrode	32
gate pad	6
source pad	6
a gate insulating film on said surface of said substrate	27
gate insulating film	27
insulating film	27
a semiconductor layer on said portion of said gate insulating film	29
semiconductor layer	29
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a source electrode and a drain electrode on said semiconductor layer	32
source electrode	32
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exposing said gate pad portion	35
exposing	35
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patterning to form an active layer	43
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Ex. L-5 LGD US PATENT No. 5,825,449

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	PAGE
active layer	39
selectively etching	43
patterning a pixel electrode electrically connected to said drain electrode	43
electrically connect/electrically connecting/electrically connected	39

EXHIBIT L-5 U.S. PATENT NO. 5,825,449 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A wiring structure comprising:
- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

- a second conductive layer formed on a first portion of said first insulative layer;
- a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;
- an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

LGD's Claim Construction

conductive layer¹ – thickness of electrically conductive material

connected to² – directly connected to

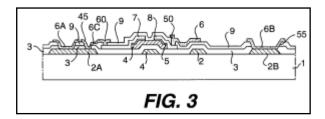
one of said first and second conductive layers – one, but not both, of the first and second conductive layers

one – a single layer

¹ Disputed Term "conductive layer" also appears in asserted claims 10 and 11 in the same context.

² Disputed Term "connected to" also appears in asserted claim 11 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERM "CONDUCTIVE LAYER":



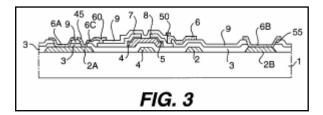
deposited. As a result, since both the first (45) and fourth (60) contact holes are formed over source pad 2A (formed of the same material as the gate) and source electrode 7, respectively, the source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer 6C connects source electrode 7 with source pad 2A, and a second transparent conductive layer 6 (i.e., the pixel electrode) is connected to drain electrode 8.

4:56-64

one end portion of each storage capacitor line 29, and connection land 32L is connected via a wire 32W to an external connection terminal 32X formed integrally with wire 32W at one marginal position of a base plate 10 (column 5, lines 6-20). Therefore, Kakuda et al. fails to disclose or suggest connection lands 29L or 32L being connected to a terminal of a thin film transistor. Thus, claim 11 is patentably distinguishable from Kakuda et al.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 6

INTRINSIC EVIDENCE FOR DISPUTED TERM "CONNECTED TO":



wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

6:8-19

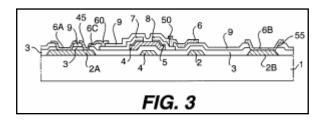
wherein one of said first and second conductive layers is connected to one of a lurality of terminals of a thin film transistor.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 2

By this Amendment, Applicant has amended claim 11 essentially to include the recitations of canceled claim 12. As amended, claim 11 recites that a wiring structure includes a third conductive layer formed on a second insulating layer and electrically connected to first and second conductive layers via first and second contact holes, wherein one of the first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor. The terminals of a thin film transistor correspond to the gate, source, and drain.

Appl. No. 08/781,188, 11/17/97 Amendment, p. 5

INTRINSIC EVIDENCE FOR DISPUTED TERMS "ONE OF SAID FIRST AND SECOND CONDUCTIVE LAYERS" AND "ONE":



wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

6.8 - 19

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

Appl. No. 08/781,188, 11/17/1997, p. 2

By this Amendment, Applicant has amended claim 11 essentially to include the recitations of canceled claim 12. As amended, claim 11 recites that a wiring structure includes a third conductive layer formed on a second insulating layer and electrically connected to first and second conductive layers via first and second contact holes, wherein one of the first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor. The terminals of a thin film transistor correspond to the gate, source, and drain.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 5

INTRINSIC EVIDENCE FOR DISPUTED TERMS "ONE OF SAID FIRST AND SECOND CONDUCTIVE LAYERS" AND "ONE" (cont'd):

one end portion of each storage capacitor line 29, and connection land 32L is connected via a wire 32W to an external connection terminal 32X formed integrally with wire 32W at one marginal position of a base plate 10 (column 5, lines 6-20). Therefore, Kakuda et al. fails to disclose or suggest connection lands 29L or 32L being connected to a terminal of a thin film transistor. Thus, claim 11 is patentably distinguishable from Kakuda et al.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 6

EXHIBIT 5 U.S. PATENT NO. 5,825,449 TERMS IN DISPUTE

ASSERTED CLAIM 10

- 10. A liquid crystal display device comprising:
- a substrate:
- a first conductive layer on said substrate including: a gate electrode,
 - a gate pad, and
- a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

gate $pad^1 - a$ portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal

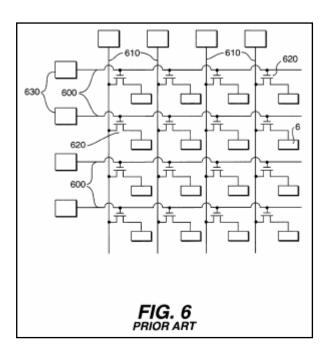
LGD's Claim Construction

source $pad^2 - a$ portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal

¹ Disputed Term "gate pad" also appears in asserted claim 11 in the same context.

² Disputed Term "source pad" also appears in asserted claim 11 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS "GATE PAD" AND "SOURCE PAD":



Case 1:06-cv-00726-JJF

Thin film transistors 620, serving as active devices, are located at intersecting portions of gate lines 600 and data lines 610. Gate lines 600 and data lines 610 are connected to the gates and sources, respectively of thin film transistors 620. In addition, pixel electrodes 6 are connected to respective drain electrodes of thin film transistors 620. Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

1:22-30

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c). Next, as shown in FIG. 1d, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode 6, which is formed on a portion of the display pixel, while ITO patterns 6A and 6B are formed on source pad 2A and gate pad 2B, respectively.

1:51-60

<u>INTRINSIC EVIDENCE FOR DISPUTED TERMS "GATE PAD" AND "SOURCE PAD" (cont'd):</u>

thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:11-15

EXHIBIT 5 U.S. PATENT NO. 5,825,449 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A wiring structure comprising:

- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

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- a second conductive layer formed on a first portion of said first insulative layer;
- a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;
- an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

LGD's Claim Construction

wiring structure – a structure electrically connecting at least two points

layer¹ – a thickness of material

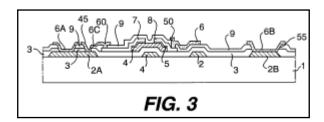
insulative layer – a thickness of non-conductive material (such as SiNx) that has a high electrical resistance

overlying² – above

¹ Disputed Term "layer" also appears in asserted claims 10 and 11 in the same context.

² Disputed Term "overlying" also appears in asserted claims 10 and 11 in the same context.

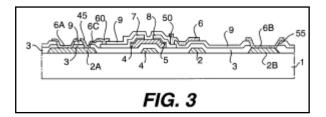
INTRINSIC EVIDENCE FOR DISPUTED TERM "WIRING STRUCTURE":



gate pad 2C. In addition, ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed.

4:22-27

INTRINSIC EVIDENCE FOR DISPUTED TERM "LAYER":



deposited. As a result, since both the first (45) and fourth (60) contact holes are formed over source pad 2A (formed of the same material as the gate) and source electrode 7, respectively, the source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer 6C connects source electrode 7 with source pad 2A, and a second transparent conductive layer 6 (i.e., the) pixel electrode) is connected to drain electrode 8.

4:56-64

one end portion of each storage capacitor line 29, and connection land 32L is connected via a wire 32W to an external connection terminal 32X formed integrally with wire 32W at one marginal position of a base plate 10 (column 5, lines 6-20). Therefore, Kakuda et al. fails to disclose or suggest connection lands 29L or 32L being connected to a terminal of a thin film transistor. Thus, claim 11 is patentably distinguishable from Kakuda et al.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 6

INTRINSIC EVIDENCE FOR DISPUTED TERM "INSULATIVE LAYER":

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped

1:39-48

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resis-

3:50-56

INTRINSIC EVIDENCE FOR DISPUTED TERM "OVERLYING":

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped semiconductor layer 5 and amorphous silicon layer 4 are then etched in accordance with a predetermined active layer pattern.

1:39-50

EXHIBIT 5 U.S. PATENT NO. 5,825,449 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A wiring structure comprising:
- a substrate;
- a first conductive layer formed on a first portion of said
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;



- a second conductive layer formed on a first portion of said first insulative layer;
- a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;
- an indium tin oxide layer formed on said second insulative layer,
- wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and
- wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

LGD's Claim Construction

formed on a first portion of said substrate - above and in contact with a first part of the substrate

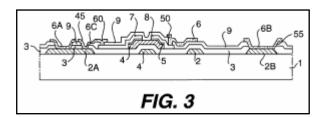
formed on – above and in contact with

formed on a second portion of said substrate - above and in contact with a second part of the substrate

formed on a first portion of said first insulative layer above and in contact with a first part of the first insulative layer

formed on said second conductive layer and on a second portion of said first insulative layer overlying said **first conductive layer** – above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "FORMED ON . . . ":



As shown in FIG. 1a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, storage capacitor electrode 2D, source pad 2A, and gate pad 2B. Gate pad 2B is used for receiving a voltage to drive and active layer in the completed TFT device.

1:34-39

In other words, a conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate



pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

4:56-5:5

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

6:3-5

ASSERTED CLAIM 1

- A wiring structure comprising:
- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

- a second conductive layer formed on a first portion of said first insulative layer;
- a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;
- an indium tin oxide layer formed on said second insulative layer,
- wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and
- wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

LGD's Claim Construction

contact hole¹ – an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection

provided through² – the contact hole is formed in the layer

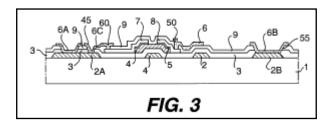
expose part of said ... layer – removing portions of one or more layers to uncover at least part of another layer

extends through – is disposed in

¹ Disputed Term "contact hole" also appears in asserted claims 10 and 11 in the same context.

² Disputed Term "provided through" also appears in asserted claim 10 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS "CONTACT HOLE", "PROVIDED THROUGH" AND "EXTENDS THROUGH":



To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

2.37-55

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

3:1-14

INTRINSIC EVIDENCE FOR DISPUTED TERMS "CONTACT HOLE", "PROVIDED THROUGH" AND "EXTENDS THROUGH" (cont'd):

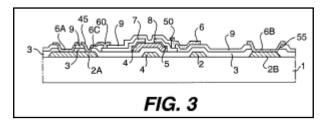
As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:6-15

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

5:6-15

INTRINSIC EVIDENCE FOR DISPUTED TERM "EXPOSE PART OF **SAID...LAYER":**



To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

2.37-55

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

3:1-14

INTRINSIC EVIDENCE FOR DISPUTED TERM "EXPOSE PART OF SAID . . . LAYER" (cont'd):

As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:6-15

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

5:6-15

ASSERTED CLAIM 1

- A wiring structure comprising:
- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

- a second conductive layer formed on a first portion of said first insulative layer;
- a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;
- an indium tin oxide layer formed on said second insulative layer,
- wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

LGD's Claim Construction

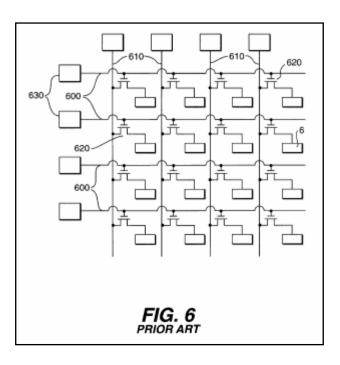
one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film **transistor** – one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor

one of a plurality of terminals of a thin film transistor – one of the terminals (i.e., source, drain, or gate) of a thin film transistor

a plurality of terminals of a thin film transistor - the terminals (i.e., source, drain, or gate) of a thin film transistor

thin film transistor - a three terminal device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "PLURALITY OF TERMINALS AT A THIN FILM TRANSISTOR":



Thin film transistors 620, serving as active devices, are located at intersecting portions of gate lines 600 and data lines 610. Gate lines 600 and data lines 610 are connected to the gates and sources, respectively of thin film transistors **620.** In addition, pixel electrodes 6 are connected to respective drain electrodes of thin film transistors 620. Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

1:22-30

As shown in FIG. 1f, a nitride film is deposited on the entire surface of the substrate as a passivation layer 9 in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer 9 is selectively etched to expose source-pad 2A and gate pad 2B, thereby completing the TFT.

2:5-10

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "PLURALITY OF TERMINALS AT A THIN FILM TRANSISTOR" (cont'd):

As shown in FIG. 2e, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode 6. As further shown in FIG. 2e, pixel electrode 6 is connected to the upper portion of drain electrode 8 At the same time, ITO pattern 6B is formed on gate pad 2C. In addition, ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed.

4:16-27

By this Amendment, Applicant has amended claim 11 essentially to include the recitations of canceled claim 12. As amended, claim 11 recites that a wiring structure includes a third conductive layer formed on a second insulating layer and electrically connected to first and second conductive layers via first and second contact holes, wherein one of the first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor. The terminals of a thin film transistor correspond to the gate, source, and drain.

App. 08/781,188, 11/17/1997 Amendment, p. 5

ASSERTED CLAIM 10

10. A liquid crystal display device comprising:

- a substrate;
- a first conductive layer on said substrate including:
 - a gate electrode,
 - a gate pad, and
 - a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation

 layer and said gate insulating film exposing said gate

 pad:
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

LGD's Claim Construction

liquid crystal display device¹a type of display that generates
an image by directing light
through an array of liquid
crystal pixels, where the
amount of light effused by each
pixel is controlled via an
electric field varying the

orientation of the liquid crystal

molecules contained within

the pixel

passivation layer – a thickness of insulative material that provides protection such as electrical stability and chemical isolation

¹ Disputed Term "liquid crystal display" also appears in asserted claim 11 in the same context.

<u>INTRINSIC EVIDENCE FOR DISPUTED TERM "LIQUID CRYSTAL DISPLAY DEVICE":</u>

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. 6, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode 6 disposed on a bottom plate. The bottom plate further includes a plurality of gate lines 600 intersecting a plurality of data lines 610.

1:13-20

7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6. The signal is stored in the form of charge on pixel electrode 6, thereby driving the liquid crystal.

2:1-4

INTRINSIC EVIDENCE FOR DISPUTED TERM "PASSIVATION LAYER":

As shown in FIG. 1f, a nitride film is deposited on the entire surface of the substrate as a passivation layer 9 in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer 9 is selectively etched to expose source-pad 2A and gate pad 2B, thereby completing the TFT.

2:5-10

As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:6-15

ASSERTED CLAIM 10

- A liquid crystal display device comprising: a substrate;
- a first conductive layer on said substrate including: a gate electrode,
 - a gate pad, and
 - a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

~

- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

LGD's Claim Construction

a gate insulating film on said surface of said substrate – a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor above and in contact with at least part of the surface of the substrate

gate insulating film – a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor

insulating film¹ – a thickness of non-conductive material (such as SiNx) that has high electrical resistance

¹ Disputed Term "insulating film" also appears in asserted claim 11 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "GATE INSULATING FILM" AND "INSULATING FILM":

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped

1:39-48

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resis-

3:50-56

ASSERTED CLAIM 10

10. A liquid crystal display device comprising:

- a substrate;
- a first conductive layer on said substrate including:
 - a gate electrode,
 - a gate pad, and
 - a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

LGD's Claim Construction

a semiconductor layer on said portion of said gate insulating

film – a thickness of semiconductor material above and in contact with a part of the gate insulating film

semiconductor layer¹ – a thickness of semiconductor material, such as amorphous silicon

impurity-doped semiconductor layer² – a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity

¹ Disputed Term "semiconductor layer" also appears in asserted claim 11 in the same context.

² Disputed Term "impurity-doped semiconductor layer" also appears in asserted claim 11 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "SEMICONDUCTOR LAYER":

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped semiconductor layer 5 and amorphous silicon layer 4 are then etched in accordance with a predetermined active layer pattern.

1:39-50

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of

2:37-47

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

2.56-67

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "SEMICONDUCTOR LAYER" (cont'd):

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer 5 is formed on amorphous silicon layer 4, as an ohmic contact layer. Impurity-doped semiconductor layer 5 and amorphous silicon layer 4 are etched according to a predetermined active layer pattern.

3:50-62

pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

5:1-5

ASSERTED CLAIM 10

10. A liquid crystal display device comprising:

- a substrate;
- a first conductive layer on said substrate including: a gate electrode,
 - a gate pad, and

 - a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation layer and said gate insulating film exposing said gate
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

LGD's Claim Construction

gate electrode¹ – a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode

a source electrode and a drain electrode on said **semiconductor laver** – a source electrode and a drain electrode above and in contact with the semiconductor layer

source electrode² - a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode

drain electrode 3 – a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode

¹ Disputed Term "gate electrode" also appears in asserted claim 11 in the same context.

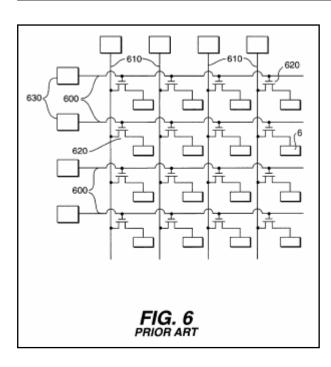
² Disputed Term "source electrode" also appears in asserted claim 11 in the same context.

³ Disputed Term "drain electrode" also appears in asserted claim 11 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "GATE ELECTRODE," "SOURCE ELECTRODE," AND "DRAIN ELECTRODE":

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

Abstract, p. 1



Thin film transistors 620, serving as active devices, are located at intersecting portions of gate lines 600 and data lines 610. Gate lines 600 and data lines 610 are connected to the gates and sources, respectively of thin film transistors 620. In addition, pixel electrodes 6 are connected to respective drain electrodes of thin film transistors 620. Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. 1a-1f.

1:22-33

INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO "GATE ELECTRODE," "SOURCE ELECTRODE," AND "DRAIN ELECTRODE" (cont'd):

As shown in FIG. 1f, a nitride film is deposited on the entire surface of the substrate as a passivation layer 9 in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer 9 is selectively etched to expose source-pad 2A and gate pad 2B, thereby completing the TFT.

2:5-10

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode,

2:56-62

Referring first to FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

3.44-49

As shown in FIG. 2e, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode 6. As further shown in FIG. 2e, pixel electrode 6 is connected to the upper portion of drain electrode 8 At the same time, ITO pattern 6B is formed on gate pad 2C. In addition, ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed.

4:16-27

ASSERTED CLAIM 10

- 10. A liquid crystal display device comprising:
- a substrate;
- a first conductive layer on said substrate including:
 - a gate electrode,
 - a gate pad, and
 - a source pad;
- a gate insulating film on said surface of said substrate,
- a portion of said gate insulating film overlying said gate electrode;
- a semiconductor layer on said portion of said gate insulating film;
- an impurity-doped semiconductor layer on said semiconductor layer;
- a source electrode and a drain electrode on said semiconductor layer;
- a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;
- a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

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- a second contact hole provided through said passivation layer exposing said drain electrode;
- a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;
- a fourth contact hole provided through said passivation layer exposing said source electrode;
- a pixel electrode electrically connected with said drain electrode via said second contact hole; and
- a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

LGD's Claim Construction

exposing said gate pad
[portion]¹ – removing portions
of one or more layers to
uncover at least part of a
gate pad [portion]

exposing² – removing portions of one or more layers to uncover at least part of another layer

pixel electrode³— a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device

transparent conductive layer ⁴– a thickness of transparent electrically conductive material

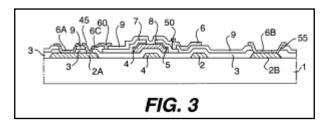
¹ Disputed Term "exposing said gate pad portion" appears in claim 11 in the same context as "exposing said gate pad" appears in claim 10.

² Disputed Term "exposing" also appears in asserted claim 11 in the same context.

³ Disputed Term "pixel electrode" also appears in asserted claim 11 in the same context.

⁴ Disputed Term "transparent conductive layer" also appears in asserted claim 11 in the same context.

<u>INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO</u> "EXPOSING":



To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

2.37-55

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connected with the source electrode through the first and fourth contact holes.

3:1-14

<u>INTRINSIC EVIDENCE FOR DISPUTED TERMS PERTAINING TO</u> "EXPOSING" (cont'd):

As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:6-15

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

5:6-15

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c). Next, as shown in FIG. 1d, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode 6, which is formed on a portion of the display pixel, while ITO patterns 6A and 6B are formed on source pad 2A and gate pad 2B, respectively.

1:51-60

7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6. The signal is stored in the form of charge on pixel electrode 6, thereby driving the liquid crystal.

2:1-4

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode 6 connected to drain electrode 8 through the contact hole overlying drain electrode 8 in the pixel part. At the same time, ITO patterns 6A, 6B and 6C are formed to contact source pad 2A and gate pad 2B through the contact holes formed at gate insulating film 3 and passivation layer 9.

5:16-22

ASSERTED CLAIM 11

LGD's Claim Construction

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole:

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

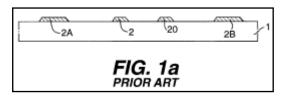
patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes. a method of manufacturing a liquid crystal display device – a process for producing a liquid crystal display device

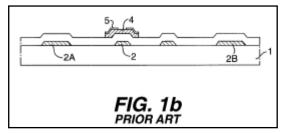
active layer – a discrete portion of semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode

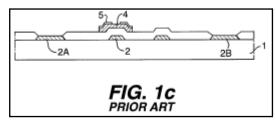
electrically
connect/electrically
connected¹ – provide an
electrical conduction path

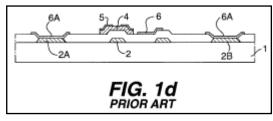
¹ Disputed Terms "electrically connect/electrically connecting/electrically connected" also appear in asserted claims 1 and 11 in the same context.

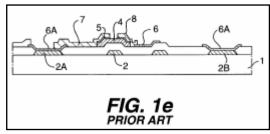
INTRINSIC EVIDENCE FOR DISPUTED TERM "A METHOD OF MANUFACTURING A LIQUID CRYSTAL DISPLAY DEVICE":

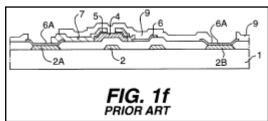












A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. 1a-1f.

1:31-33

INTRINSIC EVIDENCE FOR DISPUTED TERM "ACTIVE LAYER":

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped semiconductor layer 5 and amorphous silicon layer 4 are then etched in accordance with a predetermined active layer pattern.

Case 1:06-cv-00726-JJF

1:40-50

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impuritydoped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

2:56-67

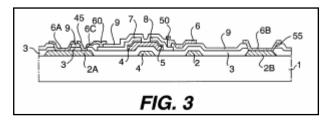
As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer 5 is formed on amorphous silicon layer 4, as an ohmic contact layer. Impurity-doped semiconductor layer 5 and amorphous silicon layer 4 are etched according to a predetermined active layer pattern.

3:50-62

pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

5:1-5

INTRINSIC EVIDENCE FOR DISPUTED TERM "ELECTRICALLY CONNECT/ELECTRICALLY CONNECTING/ELECTRICALLY CONNECTED":



wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

6:9-16

By this Amendment, Applicant has amended claim 11 essentially to include the recitations of canceled claim 12. As amended, claim 11 recites that a wiring structure includes a third conductive layer formed on a second insulating layer and electrically connected to first and second conductive layers via first and second contact holes, wherein one of the first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor. The terminals of a thin film transistor correspond to the gate, source, and drain.

Appl. No. 08/781,188, 11/17/1997 Amendment, p. 5

ASSERTED CLAIM 1

Case 1:06-cv-00726-JJF

LGD's Claim Construction

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film; forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes. patterning... to form an active layer – the removal of selected portions of the impurity-doped semiconductor layer and the semiconductor layer using etching techniques in order to form an active layer

patterning – the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material

selectively etching – the removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface

patterning a pixel electrode electrically connected to said drain electrode – the removal of selected portions of a pattern of transparent electrically conductive material to form a pixel electrode that has an electrical conduction path with the drain electrode

INTRINSIC EVIDENCE FOR DISPUTED TERMS "PATTERNING ... TO FORM AN ACTIVE LAYER" AND "PATTERNING":

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impuritydoped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

2:56-67

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer 5 is formed on amorphous silicon layer 4, as an ohmic contact layer. Impurity-doped semiconductor layer 5 and amorphous silicon layer 4 are etched according to a predetermined active layer pattern.

3:50-62

As shown in FIG. 2e, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode 6. As further shown in FIG. 2e, pixel electrode 6 is connected to the upper portion of drain electrode 8 At the same time, ITO pattern 6B is formed on gate pad 2C. In addition, ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed.

4:16-27

INTRINSIC EVIDENCE FOR DISPUTED TERM "SELECTIVELY ETCHING":

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

3:1-14

As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed pads 7A and 2C.

4:6-15

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

5:5-15

INTRINSIC EVIDENCE FOR DISPUTED TERM "PATTERNING A PIXEL ELECTRODE ELECTRICALLY CONNECTED TO SAID DRAIN ELECTRODE":

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c). Next, as shown in FIG. 1d, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode 6, which is formed on a portion of the display pixel, while ITO patterns 6A and 6B are formed on source pad 2A and gate pad 2B, respectively.

1:51-60

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impuritydoped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a



source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

2:56-3:14

INTRINSIC EVIDENCE FOR DISPUTED TERM "PATTERNING A PIXEL ELECTRODE ELECTRICALLY CONNECTED TO SAID DRAIN ELECTRODE" (cont'd):

Referring first to FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

3:44-49

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer 5 is formed on amorphous silicon layer 4, as an ohmic contact layer. Impurity-doped semiconductor layer 5 and amorphous silicon layer 4 are etched according to a predetermined active layer pattern.

3:50-62

As shown in FIG. 2c, a conductive layer for forming source electrode 7 and drain electrode 8 is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer 5 are

3:63-67

INTRINSIC EVIDENCE FOR DISPUTED TERM "PATTERNING A PIXEL ELECTRODE ELECTRICALLY CONNECTED TO SAID DRAIN ELECTRODE" (cont'd):

In other words, a conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate

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pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

4:65-5:15

EXHIBIT L-6(a)

Document 389-12 Case 1:06-cv-00726-JJF Filed 08/12/2008 Page 2 of 20 1 **Priority** SCANNED Send 2 FILED Enter CLERK, U.S. DISTRICT COURT Closed 3 JS-5/JS-6 **JS-2/JS-3** MAY = 5 20054 Scan Only_ 5 CENTRAL DISTRIC CALIFORNIA DEPUTY 6 7 UNITED STATES DISTRICT COURT 8 CENTRAL DISTRICT OF CALIFORNIA 9 WESTERN DIVISION 10 11 LG PHILIPS LCD CO., LTD., No. CV 02-6775 CBM (JTLx) 12 Plaintiff ORDER RE CLAIM 13 CONSTRUCTION 14 TATUNG CO. OF AMERICA, DOCKETED ON CM TATUNG COMPANY and 15 CHUNGHWA PICTURE TUBES, LTD. 16 MAY - 9 2005 Defendants. 17 18 The matter before the Court is claim construction regarding the side-mount 19 patents and semiconductor patents. The claim construction hearing occurred on 20 January 13-14, 2005, the Honorable Consuelo B. Marshall presiding. 21 **JURISDICTION** 22 This Court has jurisdiction pursuant to 28 U.S.C. §1331. 23 FACTUAL AND PROCEDURAL BACKGROUND 24 L.G. Philips LCD Co, Ltd. ("LPL") filed this action on August 29, 2002, 25 alleging that Defendants Tatung Co., Tatung Co. of America, and Chunghwa 26 Picture Tubes ("CPT") infringed on its patents. On December 20, 2002, CPT 27 filed an Answer and Counterclaims. On August 31, 2004, this Court-granted in 28 part CPT's motion for leave to amend its Answer and Counterclaims and to J

LGE as a party. On October 12, 2004, this Court denied LPL's motion to stay further proceedings pertaining to the side-mount patents and set the claim construction hearing for January 7, 2005. On its own motion, the Court continued the claim construction hearing to January 13, 2005.

LEGAL STANDARD

In interpreting an asserted claim, the Court first looks to the intrinsic evidence, i.e., the patent itself, including the claims, the specification and, if in evidence, the prosecution history." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576 (Fed. Cir. 1996). However, all intrinsic evidence is not equal. First, the Court should focus on the claims themselves, both asserted and unasserted, to define the meaning and scope of the patented invention. *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1201-02 (Fed. Cir. 2002). There is a "heavy presumption" that the ordinary and accustomed meaning of a claim term, as understood by one of ordinary skill in the art, is the correct construction. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). Dictionaries, encyclopedias and treatises, which are extrinsic evidence, may be employed to "assist the court in determining the ordinary and customary meanings of claim terms." *Texas Digital*, 308 F.3d at 1202.

Second, the Court should review the specification. *Vitronics*, 90 F.3d at 1582. A review of the specification will reveal whether or not the inventor has given a term an unconventional meaning. *Id.* However, it is improper to read a limitation into a claim from the specification. *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182 (Fed. Cir. 1998). The inventor may act as his or her own lexicographer and use terms in a manner other than their ordinary meaning, so long as any such specific definition is clearly stated in the patent specification or prosecution history. *Mycogen Plant Science Inc. v. Monsanto Co.*, 243 F.3d 1316, 1327 (Fed. Cir. 2001). Therefore, for claim construction purposes, the specification is "the single best guide to the meaning of a disputed term."

Vitronics, 90 F.3d at 1582.

Third, the Court may consider the prosecution history of the patent. The prosecution history is significant because it reveals "the course of dealing with the Patent Office, which may show a particular meaning attached to the terms, or a position taken by an applicant" to secure the patent. *Markman*, 52 F.3d at 991. As such, the prosecution history may be reviewed to assess whether a patentee "relinquished [a] potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a [prior art] reference." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999), *cert. denied*, 529 U.S. 1066 (2000). However, for subject matter to be held relinquished, a court must find that the patentee disclaimed the subject matter with "reasonable clarity and deliberateness." *Northern Telecom Ltd. v. Samsung Electronics Co., Ltd.*, 215 F.3d 1281, 1294 (Fed. Cir. 2000).

Finally, if and only if a claim remains "genuinely ambiguous" despite the full consideration of the intrinsic evidence, then a court may look toward extrinsic evidence to interpret the claim term itself. *Bell & Howard Document Mgmt*.

Prods. Co. v. Altek Sys., 132 F.3d 701, 706 (Fed. Cir. 1997). The need for such a departure from the intrinsic evidence "rarely, if ever, occurs." Vitronics, 90 F.3d at 1585.

ANALYSIS

A. Side-Mounting Patents

The side-mounting patents consist of U.S. Patents Nos. 6,373,537 ('537 patent), 6,00,457 ('457 patent), 6,020,942 ('942 patent), and 5,926,237 ('237 patent).

1. Whether the Side-Mounting Patents Are Limited to Portable Computers

The definition of the terms "liquid crystal display," "liquid crystal panel," "housing" and "outer casing" are disputed because CPT limits them to "portable

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computers" whereas LPL does not so limit them. The '537 and '237 patents whereas the '457 patent contains claims directed only to the LCD device and the '942 patent contains claims. '942 patent contains claims directed only to a portable computer. Since the Court must look first to the claims, the Court finds that claims that recite a "portable computer" are limited to portable computers, but claims that do not recite a "portable computer" are not so limited. The background of the invention also indicates that the portable computer is an example of a device that uses an LCD. See, e.g., 1:50-51 ("[t]he liquid crystal display is usually combined with, for example, a notebook computer for use as an output screen"; 1:59-61 ("a liquid crystal display is attached to a device such as a notebook computer"). With respect to the terms "housing" and "outer casing," the Court notes that independent claims, such as Claim 37 of the '457 patent, which contain the term "housing" do not contain the words "portable computer," whereas dependent claim 40 of the '457 patent states "the housing includes a portable computer." This indicates that the definition of the terms should not be limited to a portable computer.

Defendants look at the specification, rather than first looking to claims, in arguing that the invention described in the specification is directed to an improvement for a portable computer. Defendants' argument is not persuasive, as the Federal Circuit has held that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004); *accord Gemstar-TV Guide Int'l Inc. v. ITC*, 383 F.3d 1352, 1366 (Fed. Cir. 2004). The specification of the sidemounting patents does not contain any "clear disavowal" of products that are not portable computers. In addition, this Court rejects Defendant's argument that the

sidemounting patents should be limited to portable computers because that was the purported "object" of the invention. "The fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives." Liebel, 358 F.3d at 908. See also Ex-Pass Tech, Inc. v. 3Com Corp., 343 F.3d 1364, 1370 (Fed. Cir. 2003) ("The Court's task is not to limit claim language to exclude particular devices because they do not serve a perceived "purpose" of the invention."). Thus, the Court adopts LPL's definitions of the terms "liquid crystal display," "liquid crystal panel", "housing" and "outer casing."

2. Whether Constructions Should Include the Word "Directly"

The word "directly" does not appear anywhere in the claim language. However, Defendants use the word "directly" in construing the terms "attachable to a housing," "fixable to a housing," "joined with," "joining together," "coupled," and "fastening part." Defendants argue that the claim language, in context, indicates that side-to-side direct connection must be present, as the specification does not show any intervening element. The Court finds Defendants' arguments unpersuasive pursuant to *Liebel*, which makes it clear that the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction. Since no such words of manifest exclusion or restriction are used here, the Court adopts LPL's definitions of "attachable to a housing" or "fixable to a housing," "joined," "joined together," "coupled," and "fastening part."

3. Whether the terms "through" and "passing through" should have different meanings

LPL proposes that the term "through" be used in its plain and ordinary way to mean "by way of," and that "passing through" means "extending into."

Defendants contend that "through" means "in at one end, side or surface and out

the other" and that "passing through" means "moving past or making way in one side and out of the other side." Although the preferred embodiment shown in the drawings uses screws engaging holes to connect the components, the patent clearly contemplates other methods of attaching the components. The '457 patent specification, for example, provides that "an adhesive device, such as double-sided tape can be used instead of the second and third screw holes" and that "the rear case 500 and the second support frame 400 are jointed to each other using hooks and/or other suitable fastening devises, including adhesives." See, e.g., 4:58-60, 4:63-67. Since LPL's definition of "through" covers both screws and adhesives, the Court finds that it is the better definition.

LPL contends that the phrase "passing through," in contrast to "through," is used only in reference to screws and screw holes, which extend into an object. CPT, on the other hand, argues that "passing through" and "through" have the same meaning. The doctrine of claim differentiation indicates that different words or phrases used in different claims are presumed to indicate that the claims have different meaning and scope. *Karlin Tech, Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 971 (Fed. Cir. 1999). Here, it appears that the inventors used the term "through" when generally referring to a fastening part but used "passing through" only when referring to a specific fastening part (i.e., a screw). Therefore, the Court adopts LPL's definitions of "through" and "passing through."

4. Whether the terms "frame," "first frame," and "second frame" should be given their plain and ordinary meanings.

LPL defines "frame" to mean "a support structure." Defendants defines "Frame" as "an open structure or rim for encasing, holding or bordering that encloses a substantial portion of each side edge of another structure." Defendants base their argument on the theory that the meaning of the word "frame" is limited to the description in the specification. Under *Liebel*, this restrictive interpretation is inappropriate. Furthermore, Defendants define "first" and "second" frame to

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mean "inner" and "outer" frame, even though the inventors did not use those terms. The use of "first" and "second" follow the "common patent-law convention to distinguish between repeated instances of element or limitation." 3M Innovative Properties Co. v. Avery Dennison Corp., 350 F.3d 1365, 1371 (Fed. Cir. 2003). For example, Claim 31 of the '942 patent claims "[t]he portable computer according to claim 13 wherein the fastening part includes first and second screws passing through first and second holes at a same side edge of at lease one of the first and second frames." 8:25-28. Here, the words "first" and "second" are consistently used to distinguish repeated instances of element or limitation. Therefore, the Court gives "frame," "first frame" and "second frame" their ordinary meanings, as set forth by LPL.

5. Whether "liquid crystal display model" is a typographical error

The parties agree on the construction of the claim term "liquid crystal display module." However in one claim, Claim 7 of the '537 patent, the term appears as "liquid crystal display model." Given the context, this is clearly a typographical error. Other parts of Claim 7 refer to the "liquid crystal display module." The Court therefore construes "liquid crystal display model" as "liquid crsytal display module."

6. Whether Definitions are Needed for "Portable Computer," "Side", "Forming" and "Cover"

Defendants propose cumbersome definitions for the terms "portable computer," "side", "forming" and "cover." The Court finds that these definitions create unnecessary confusion and adopts LPL's constructions, which give the terms their plain and ordinary meaning.

B. Construction of the '737 Semiconductor Patent

1. "Source Electrode," "Drain Electrode," and "Gate Electrode"

While LPL construes the electrode to include the line and the pad, Defendants limits the electrode to a single TFT and construes the electrodes as

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distinct from the lines and the pads. The seventh step of claim 1 of the '737 patent calls for "exposing a part of each of said source electrode, drain electrode and gate electrode." LPL persuasively argues that electrodes are exposed at the pad region for electrical connection, as exposing a gate pad allows electrical control of all TFT gate contacts along the row. One of ordinarily skill would not control each TFT gate/source independently, especially since creating a hole at each TFT to expose the gate electrode would destroy the TFT. Furthermore, the specification of the '737 patent describes a step in which "gate electrode 2 extending along one line and gate electrodes 2' on another line are formed on a transparent insulating substrate 1 such as glass substrate." 3:25-28. This indicates that a structure separate from the TFT is part of the "gate electrode." In addition, the claims in the application for the '449 patent include phrases such as "said pad comprising: a portion of said data electrode" and "a pad including a portion of [said] data electrode." Finally, U.S. Patent 4,705,358 ('358 patent), which also pertains to the same technology as the '737 patent, names the same inventor as the '737 patent, and was filed in the U.S. on the same day as the '737 patent, illustrates a gate electrode from above (i.e. a "bird's-eye-view") and demonstrates that the "gate electrode" may include the gate line. The Court therefore finds that the electrodes may include the lines and pads. Furthermore, the Court is not persuaded by that portion of Defendant's construction which specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Continuously Depositing"

LPL construes the term "continuously depositing" as "[t]he formation of the gate insulting film, the high-resistivity semiconductor film and conducting film without intervening films." Defendants offer a modified construction of this term

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as meaning that "the deposition of the specified films occurs without any nondeposition related steps between or during the deposition of each constituted film." While LPL's definition requires the films to be only spatially continuous. Defendants' definition requires continuity in space, time and sequence. The '737 patent shows "continuously deposited" films as being spatially continuous, but it does not show, mention or require the deposition to be performed without an interruption in time or sequence. Moreover, the plain meaning of "continuous" is "uninterrupted extension in space, time or sequence." The Court therefore adopts LPL's construction of "continuously depositing."

3. "Oxidizing atmosphere"

Claim 1 of the '737 patent requires "continuously depositing [the films]... without exposing them to an oxidizing atmosphere." LPL construes "an oxidizing atmosphere" as "an atmosphere that would create substantial oxidation on a film." The Court finds that the word "substantial" in this construction is vague and ambiguous. Defendants initially construed this phrase to mean that the films are not permitted to be exposed to "an oxide," although they acknowledged that a de minimus amount of oxidation is not an "oxidation atmosphere." Defendants subsequently modified their construction to be "an atmosphere that would create a detectable amount of oxidation on a film." As "detectable" is more precise than "substantial," the Court adopts Defendants' modified construction of this term.

4. "Island region"/ "island region on said gate electrode"

At the time the patent application was filed, there were at least two wellknown constructs for the semiconductor region in a TFT. In one design, separate islands of semiconductor are created above each TFT's gate electrode. In the other design, a single, unitary semiconductor region extends over all of the TFTs in one large "continent." While LPL construes the term "island region" as used in the '737 patent to include both designs, Defendants' construction limits this term to the first design (i.e. a region located over the gate electrode of a single TFT).

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Defendants also require the island to have been "etched around its entire perimeter."

SCAMNED Defendants' argument is persuasive, as claim 1 recites a process for producing "a thin-film transistor." 4:26. See also 1:5, 13, 29, 57, 65, 67; 2:9; 3:34-35. Furthermore, in discussing FIG. 3b, the specification provides that "said low-resistivity amorphous silicon film 20 and high-resistivity amorphous silicon film 4 are left as an island region in the area where a thin-film transistor is to be formed." 3:34-35. This statement indicates that the "island region" is limited to the area of a single TFT and does not include multiple TFTs. Thus, the Court finds that Defendants' construction more accurately reflects the language of the claim and the specification. Moreover, LPL's construction appears to read the term "island region" completely out of the third step, "in which said highresistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode." The Court therefore adopts Defendants' construction of the term "island region."

5. "Conducting Film Containing at Least a low-resistivity Semiconductor Film"/ "Conducting Film"/ "High-resistivity Semiconductor Film"/ "Low-Resistivity Semiconductor Film"

The '737 patent discloses two preferred embodiments. One embodiment includes four continuously deposited films: an insulating film, a high-resistivity semiconductor films, a low-resistivity semiconductor film, and a conducting film. See 2:17-21, Fig. 2a-2e. The other embodiment has three continuously deposited films: an insulating film, a high-resistivity semiconductor films, and a lowresistivity semiconductor film. See 2:24-30, Fig. 3a-3d.

Claim 1 of the '737 patent sets forth "a second step for continuously depositing . . . a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low -resistivity semiconductor film." Claim 2, which is not at issue in this litigation, sets forth a second step wherein "said

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conducting film is composed of at least two layers consisting of a low-resistivity semiconductor films and thereon a refractory metal film or transparent conducting film."

According to LPL, the italicized phrase in Claim 1 above means that the conducting film may consist only of a low-resistivity semiconductor film. CPT, on the other hand, construes this phrase as requiring a conducting film with adjoining layer of low resistivity semiconductor and possibly other adjoining layers. CPT relies on a sentence in the specification discussing Fig. 3a-3d, which states that, "[i]n this example, no conducting film is formed on low-resistivity amorphous silicon film 20, but a conducting film such as ITO film may be formed on said low-resistivity film 20 as in the example shown in FIG. 2." While this sentence does suggest that the conducting film is distinct from the low-resistivity semiconductor film, CPT's interpretation would narrow the scope of Claim 1 to exclude the second embodiment. A claim construction that excludes a preferred embodiment is "rarely, if ever, correct." Dow Chemical Co. v. Sumitomo Chemical Co., 257 F.3d 1364, 1378 (Fed. Cir. 2001). Furthermore, the fact that the conducting film is specifically described as having two layers in claim 2 but not in claim 1 indicates that two adjoining layers are not needed for the first claim. Thus, the Court adopts LPL's construction of the term "conducting film containing at least a low-resistivity semiconductor film."

LPL's construction of "conducting film" is consistent with this Court's determination that the conducting film can be the low -resistivity semiconductor film. LPL construes "conducting film" according to its plain meaning, namely, a thickness of electrically conductive material. Defendants' construction of conducting film, on the other hand, restricts it to film "having an electrical

¹LPL submits intrinsic evidence in the form of a scientific article describing ITO (indium tin oxide) as a "semiconductor." This supports LPL's position that the conducting film can be the lowresistivity semiconductor.

resistance several order of magnitude lower than a low-resistivity semiconductor film." In other words, Defendants define "conducting film" as distinct from "low-resistivity semiconductor film." The Court rejects Defendants' construction and adopts LPL's construction since it finds that the conducting film in claim 1 of the '737 patent may consist of the low-resistivity semiconductor film, as discussed above.

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LPL's constructions of "high-resistivity semiconductor film" and "low-resistivity semiconductor film" distinguishes these terms based on their relative resistivity. Defendants distinguish the terms according to whether they are "doped" (i.e. intentionally mixed with impurities) or "undoped." The '737 patent makes no mention of the terms "doped" and "undoped." Furthermore, LPL presents evidence that it is improper to equate the terms high-resistivity with "undoped" and low-resistivity with "doped." The Court therefore rejects Defendants' method of distinguishing these terms. Defendants also rely solely on extrinsic evidence in defining high-resistivity semiconductor film as having a resistence "many orders of magnitude" greater than the low-resistivity film. The Court finds this language vague and unnecessary. The Court therefore adopts LPL's constructions of the terms "high-resistivity semiconductor film" and "low-resistivity semiconductor film."

6. "Mask"/ "At least a part of the Mask"/ "Said source and drain electrodes serving as at least part of the mask"

Claim 1 requires a step for selectively removing material "with said source and drain electrodes serving as at least part of the mask." The parties dispute whether an electrode covered by photoresist serves as at least part of the mask. Defendants' construction may exclude such an electrode, as it requires that the source and drain electrodes "make a significant contribution to defining the edges of the selectively removed region" or alternatively "shield at least part of the surface from the action of the removal technique." While the photoresist may be

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the *outermost* layer of the mask, the electrodes are part of the mask structure, as, they, too, are resistive to the removal technique and in the pattern needed to etch exposed conductive film. LPL construes "mask" as "a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed." The Court finds that this definition best explains the mask, as well as how the electrodes serve as "at least a part of the mask." The Court does not need to construe "said source and drain electrodes serving as at least part of the mask," since this phrase simply combines the terms "source electrode," "drain electrode" and "at least a part of the mask."

7. "Thin Film Transistor"

LPL's and Defendants' construction of "thin film transistor" ("TFT") are very similar. They differ in one respect: LPL specifies that TFTs are not constructed in a single crystal silicon wafer. Since the single wafer is mentioned in the intrinsic evidence and Defendants do not deny that TFTs are constructed in a single crystal silicon wafer, the Court adopts LPL's construction.

8. "A fourth step for selectively forming a source electrode and drain electrode"

LPL's construction of "a fourth step for selectively forming a source electrode and drain electrode" requires the source and drain electrodes to be "formed together." The Court finds nothing in the claim or specification that supports this interpretation. Although the formation of the source and drain electrodes is listed in one step, nothing suggests that each action within each step must be performed together. LPL's argument that the objective of the invention supports this interpretation is unpersuasive in light of Liebel, discussed above. However, the Court also finds Defendants' construction problematic. Defendants construe this phrase as "forming a source electrode and drain electrode in selected regions only by depositing a conducting film or other material such as Al."

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Figures 1-3 and the specification do indicate that the source and drain electrode are formed in selected regions. See 1:15-17, 2:10-14,, 3:36-44. However, the specification does not support the second part of CPT's construction. Rather, the specification indicates that source and drain electrodes can be formed via deposition and subsequent etching of conductive material. The Court therefore modifies Defendant's construction and defines the phrase as "forming a source electrode and drain electrode in selected regions only," which is consistent with the Court's construction of "selectively forming" below.

"Contacting a part of the surface of said island region" 9.

LPL construes "contacting a part of the surface of said island region" to mean "[f]orming an electrical connection to a part of the surface of the island region" while Defendants construe it to require "touching a part of the surface of the island region." The Court finds that Defendants' construction better reflects the plain meaning of the claim.

"Forming ... on" 10.

The first step of claim 1 is "for forming a gate electrode on an insulating substrate." LPL argues that the '737 patent uses "forming" in the sense of "providing" whereas Defendants construe "forming" as to give "form or shape to." The Court finds it awkward to define "forming" as "providing" in the phrase "selectively forming a gate electrode 2 on an insulating substrate 1," which is offered as intrinsic evidence by both parties. Defendants' construction is more meaningful in this specific context as well as in the specification and the claims as a whole. Moreover, Defendant's construction is consistent with this Court' definition of "a fourth step for selectively forming a source electrode and drain electrode." The Court therefore adopts Defendants' construction of "forming... .on."

"Selectively etched"/ "Selectively forming"/ "Selectively 11. removing"

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Claim 1 recited a third step wherein "said high-resistivity semiconductor film and said conducting films are selectively etched so that they are partly left as an island region on said gate electrode." LPL defines "selectively etched" as the "removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface." Defendants object to this definition because it refers to removal of portions of a surface, rather than the entire film. While the claim does specifically refer to the etching of the high-resistivity semiconductor film and the conducting films, the Court finds nothing in the language of the claim or the specification that requires etching of the entire film. Furthermore, Defendants' construction, which requires etching of the high-resistivity semiconductor film, the conducting film, and the low-resistivity semiconductor film, is inconsistent with both the language of the claim and with this Court's finding that the conducting film may constitute the low-resistivity semiconductor film. The Court therefore adopts LPL's definition of "selectively etched."

In addition, Claim 1 recites a fourth step for "selectively forming a source electrode and a drain electrode," and a fifth step for "selectively removing said conducting film exposed on said island region." The Court finds no substantive difference between LPL's and Defendants' constructions of "selectively forming" and "selectively removing." However, the Court adopts Defendants' definitions of these respective terms as "forming in selected regions only" and "removing selected regions only" because they convey the meaning in the simplest language.

C. Construction of Disputed Terms of the '449 Patent

1. Gate Electrode/ Source Electrode

Defendants construe the gate/ source/ data electrodes to exclude the lines and pads. Claims 10 and 11 of the '449 patent do refer to the gate electrode, gate pad, source electrode, and source pad individually. For example, claim 10 recites that the liquid crystal display device is comprised of "a first conductive layer . . .

including: a gate electrode, a gate pad, and a source pad." (7:34-39). The specification, however, provides additional information that helps clarify the relationship between the electrodes and the pads. In Figures 2d and 2e, the source pad and source electrode are shown as one connected structure, although they are labeled 7 and 7A respectively. In discussing Figure 2c, the specification states that "source electrode 7 thus forms part of a transistor region and serves as source pad 7A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT." (4:1-5). In discussing Figure 2e, the specification states that "ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD." In describing the second embodiment depicted in Figure 3, the specification provides that "source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed." Thus, while the source pads and electrodes are formed separately, they are then connected and the specification's language indicates that they are not necessarily distinct structures. The originally filed application during the prosecution of the '449 patent also supports LPL's position that the electrode should not be defined as excluding the line and pad. The first claim of the original application recites "[a] pad for providing an[] electrical connection to a data electrode of a switching device, said pad comprising: a portion fo said data electrode " The fourth claim in the original application recites "a liquid crystal display device comprising: a data line; and a pad, said pad including: a portion of said data line. . . . " Likewise, the intrinsic evidence does not indicate that the gate electrode must exclude the gate pad. In fact, Figures 2a-2e do not include a separate number identifying the "gate electrode." The Court therefore rejects a construction of "electrode" that specifically excludes the line and pad.

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²The word "data" corresponds to "source."

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3. "On"/ "formed on"/ "disposed on"

The Court also rejects Defendant's construction of these terms because it specifies a particular direction for flow of charge carriers (from the source electrode toward the drain). The intrinsic evidence does not support such a limitation. Furthermore, as discussed previously with respect to the '737 patent, the embodiment shown in Figure 3 of the '737 patent illustrates an arrangement where the direction of flow is reversed. Accordingly, the Court adopts LPL's construction of "source electrode," "gate electrode," and "drain electrode."

2. "Gate pad"/ "Source pad"

According to LPL's construction, pads are provided near the periphery of the TFT array "to receive data from a [gate or data] driving circuit." Defendants contend that this is ambiguous because other parts of the wiring, which are not pads, may also receive data from an external driving circuit. Defendants construe the pads as an element "that is necessary in order to communicate information from an external driving circuit to a [gate or source] electrode." Defendants base this construction on a sentence in the specification which states that "a pad wiring" layer is necessary in order to communicate information from an external driving circuit to the gate and source." (1:51-53). Since the specification refers to the pad wiring layer as being necessary and not the pad, the Court rejects Defendants' construction and adopts LPL's constructions of "gate pad" and "source pad."

LPL defines "on", "formed on" and "disposed on" as "touching a top or side of." LPL contrasts these terms with "overlying," which it defines as "above" something but not necessarily touching it. This Court agrees with Defendants that the specification does not support the distinction made by LPL. For example, the specification states that a "conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8." (5:6-8) (emphasis added). Conductive layer 7 and 8 do not touch the substrate (see Fig. 3), yet the specification uses the word "on." See

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also 2:42-44; 3:50-54; 7:49-50 (all using the word "on" to describe a situation where there is no "touching"). The Court therefore adopts Defendants' definition of "on."

4. "Contact hole is provided through . . . layer"/ "Provided through"

The phrases "contact hole is provided through" and "provided through" appear only in claims 1 and 10, always in the context of a contact hole being "provided through" one or more layers of materials. Defendants construe the claim terms to mean that these holes are "made in one side and out the opposite side" of the layers of materials. The Court finds that these phrases should be given their ordinary meaning and therefore adopts LPL's constructions.

5. "Active layer"

Defendants' construction of "active layer" limits this area to the region of the semiconductor layer that forms the channel region between the source and drain electrodes. Figures 2b-e, 3 and 5 of the specification show the active layer 4 extending only under the source 7 and drain 8. However, as LPL points out, these figures do not in any way limit the extension of active layer 4 in the dimension perpendicular to the figure, or in other areas of the substrate not depicted in the cross-section views. Since nothing in the claim or specification limits the active layer to the region of semiconductor layer between the source and drain electrodes, the Court adopts LPL's construction of this term.

6. "Common hole"

LPL construes "common hole" in accordance with its plain meaning as "[a] shared hole." Defendants construe "common hole" to mean "single hole." The court finds Defendants' construction ambiguous, since it suggests that only one hole is permitted. The Court therefore adopts LPL's construction of this term.

7. "Aligned"

LPL construed "aligned" to mean "placed in line with," which is its ordinary meaning. Defendants, on the other hand, construe "aligned" to mean

"substantially co-axial or concentric." Defendants' definition would require the holes to be one on top of the other, whereas LPL's construction would permit the holes to be placed either side-by-side or on top of each other. Although the figures in the specification show these holes to be on top of each other as described by Defendants, the plain language of the claim should not be limited by the figures in the specification. *See Dayco Products*, 258 F.3d at 1327. The Court therefore adopts LPL's construction fo this term.

8. "Said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region"

Defendants' construction of "said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region" limits the phrase to mean that "the first and second contact holes must overlap." However, none of the embodiments disclosed in the '449 patent teaches that the hole exposing the second conductive layer (i.e. the "second hold") overlaps with the hole in the first insulative layer that exposes the first conductive layer. *See, e.g.,* Fig. 3 and Fig. 5. Since a claim construction that excludes from its scope a preferred embodiment is rarely, if ever, correct, the Court adopts LPL's construction.

9. "Wiring structure"

This term "wiring structure" appears in Claims 1-5 of the '449 patent. LPL's definition characterizes the term as a "slender structure" while Defendants refer to the layer simply as a "structure." Claim 1 begins with "A wiring structure comprising: a substrate" Since the substrate is typically a large slab of glass, which is not "slender," the Court adopts Defendants' definition of this term.

IT IS SO ORDERED

DATE: May 5, 2005

CONSUELO B. MARSHALL
UNITED STATES DISTRICT JUDGE

EXHIBIT L-6(b)

Document 389-13

Filed 08/12/2008

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Case 1:06-cv-00726-JJF

1 LG.PHILIPS LCD CO., LTD., 2 Plaintiff, 3 VS. 4 LITE-ON TECHNOLOGY CORP. and LITE-ON TECHNOLOGY 5 INTERNATIONAL INC., 6 Defendants. 7 LG.PHILIPS LCD CO., LTD., 8 Plaintiff, 9 VS. 10 TPV TECHNOLOGY, LTD, and ENVISION PERIPHERALS, INC., 11 12 Defendants. 13 LG.PHILIPS LCD CO., LTD., 14 Plaintiff, 15 VS. 16 VIEWSONIC CORPORATION, 17 Defendant. 18

Pursuant to the Court's October 1, 2003 Order regarding Claim Construction Briefing, LG.Philips LCD Co., Ltd. ("LPL"), Tatung Co. of America and Tatung Company (collectively "Tatung"), Chunghwa Picture Tubes, Ltd. ("CPT"), Jean Company, Ltd. ("Jean Co."), Lite-On Technology Corporation and Lite-On Technology International Incorporated (collectively "Lite-On"), TPV Technology, Ltd. ("TPV"), Envision Peripherals, Inc. ("Envision") and Viewsonic Corporation ("Viewsonic") submit this Second Revised Joint Claim Construction Statement consisting of Exhibits A-F.

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Exhibit A is a list of claim terms for which the parties agree on a construction concerning U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237. Exhibit A is submitted on behalf of all of the parties.

Exhibit B is a list of disputed terms from U.S. Patent Nos. 6,373,537; 6,020,942; 6,002,457; and 5,926,237, along with the parties' respective constructions and support for those constructions. Exhibit B is submitted on behalf of all of the parties.

Exhibit C is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 4,624,737. Exhibit C is submitted on behalf of all of the parties.

Exhibit D is a list of disputed terms from U.S. Patent No. 4,624,737, along with the parties' respective constructions and support for those constructions. Exhibit D is submitted on behalf of all of the parties.

Exhibit E is a list of claim terms for which the parties agree on a construction concerning U.S. Patent No. 5,825,449. Exhibit E is submitted on behalf of all of the parties.

Exhibit F is a list of disputed terms from U.S. Patent No. 5,825,449, along with the parties' respective constructions and support for those constructions. Exhibit F is submitted on behalf of all of the parties.

Exhibits A-F filed herewith will supercede Exhibits A-F of the Revised Joint Claim Construction Statement, filed on September 17, 2003 ("First Revised JCC"). In addition, all supporting exhibits filed by the parties in support of their respective positions are incorporated herein.

Defendants' submission of these proposed claim constructions and corresponding support should not be construed as an admission by any defendant that any of the claims are infringed, valid or enforceable. Defendants' submissions relate to those patents asserted against them in the various Complaints.

Furthermore, defendants' submission of these proposed claim constructions do not 1-LA750383.1

affect or waive any arguments regarding the invalidity of the patents-in-suit. The
parties preserve the right to amend and/or supplement the terms and/or
constructions in the attached claim charts as claim construction discovery continues
and as the parties continue

number of the patents-in-suit. The
parties preserve the right to amend and/or supplement the terms and/or
constructions in the attached claim charts as claim construction discovery continues
and as the parties continue

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Page 6 of 108

1	to meet and confer to reduce the n	umber of claims asserted and to reduce the
2	number of terms for the Court to c	onstrue.
3 4	Dated: December, 2003	JEFFREY N. BROWN TERESA A. MACDONALD ANN A. BYUN
5		ANTHONY C. ROTH NATHAN W. McCUTCHEON
6		MORGAN, LEWIS & BOCKIUS LLP
7		Ву
8		Jeffrey N. Brown Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
9	Dated: December 23, 2003	MARK KRIETZMAN
10		CHRISTOPHER DARROW VALERIE W. HO GREENBERG TRAURIG LLP
11	·	GREENBERG TRAURIG LLP
13		By u/h
14		Mark Krietzman Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December, 2003	TERESA M. CORBIN
16		GLENN W. RHODES CHRISTOPHER A. MATHEWS BRIAN S. Y. KIM
17		HOWREY SIMON ARNOLD & WHITE LLP
18		Ву
19		Christopher A. Mathews Attorneys for Defendants/Counterclaimants CHUNGHWA PICTURE TUBES, LTD., JEAN
20 21		CHUNGHWA PICTURE TUBES, LTD., JEAN COMPANY, LTD., LITE-ON TECHNOLOGY CORPORATION, LITE-ON TECHNOLOGY
22	•	INTERNATIONAL INCORPORATED, TPV TECHNOLOGY LTD. and ENVISION
23		PERIPHERALS, INC.
24	Dated: December, 2003	SCOTT R. MILLER TRACY R. ROMAN
25		BINGHAM McCUTCHEN LLP
26		Ву
27		Scott R. Miller Attorneys for Defendant VIEWSONIC CORPORATION
28		CORPORATION
	L-PH/1933229.1	

1	to meet and confer to reduce the ne	umber of claims asserted and to reduce the
2	number of terms for the Court to c	onstrue.
3	Dated: December 2003	JEFFREY N. BROWN
4	•	TERESA A. MACDONALD ANN A. BYUN
5		ANN A. BYUN ANTHONY C. ROTH NATHAN W. McCUTCHEON MORGAN, LEWIS & BOCKIUS LLP
6		
7		Jeffrey N. Brown
8		Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
10	Dated: December, 2003	MARK KRIETZMAN CHRISTOPHER DARROW VALERIE W. HO
11	·	VALERIE W. HO GREENBERG TRAURIG LLP
12		GREENBERG TRAURIG ELF
13		ByMark Krietzman
14		Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December 23, 2003	TERESA M. CORBIN GLENN W. RHODES
16		CHRISTOPHER A MATHEWS
17		BRIAN S. Y. KIM HOWREY SIMON ARNOLD & WHITE LLP
18		
19		By Christopher A. Mathews / BSK Christopher A. Mathews
20		Attorneys for Defendants/Counterclaimants CHUNGHWA PICTURE TUBES, LTD., JEAN COMPANY, LTD., LITE-ON TECHNOLOGY CORPORATION, LITE-ON TECHNOLOGY
21		COMPANY, LTD., LITE-ON TECHNOLOGY CORPORATION, LITE-ON TECHNOLOGY
22		INTERNATIONAL INCORPORATED, TPV TECHNOLOGY LTD. and ENVISION
23		PERIPHERALS, INC.
24	Dated: December, 2003	SCOTT R. MILLER TRACY R. ROMAN
25		TRACY R. ROMAN BINGHAM McCUTCHEN LLP
26		By
27		Scott R. Miller
28		Attorneys for Defendant VIEWSONIC CORPORATION
	, BM/4033990 a	

С	se 1:06-cv-00726-JJF Document	389-13 Filed 08/12/2008 Page 9 of 108
1	to meet and confer to reduce the n	umber of claims asserted and to reduce the
2	number of terms for the Court to c	onstrue.
3	Dated: December, 2003	JEFFREY N. BROWN
4		TERESA A. MACDONALD ANN A. BYUN
5		ANTHONY C. ROTH NATHAN W. McCUTCHEON
6		MORGAN, LEWIS & BOCKIUS LLP
7		Ву
8		Jeffrey N. Brown Attorneys for Plaintiff/Counterclaim Defendant LG.PHILIPS LCD CO., LTD.
9	Dotadi Dagambar 2002	•
10	Dated: December, 2003	MARK KRIETZMAN CHRISTOPHER DARROW
11		VALERIE W. HO GREENBERG TRAURIG LLP
12		, n
13		ByMark Krietzman
14		Attorneys for Defendants TATUNG COMPANY and TATUNG CO. OF AMERICA
15	Dated: December, 2003	TERESA M. CORBIN
16		GLENN W. RHODES CHRISTOPHER A. MATHEWS
17		BRIAN S. Y. KIM HOWREY SIMON ARNOLD & WHITE LLP
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19		Christopher A. Mathews
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21		CORPORATION LITE-ON TECHNOLOGY
22		INTERNATIONAL INCORPORATED, TPV TECHNOLOGY LTD. and ENVISION PERIPHERALS, INC.
23	Dated: December 23, 2003	.
24	2 a.c.a. 12000iii06i 23, 2003	SCOTT R. MILLER TRACY R. ROMAN
25		BINGHAM McCUTCHEN LLP
26		By San B Mills
27		'Scott R. Miller Attorneys for Defendant VIEWSONIC CORPORATION
28		CORTORATION
	1-PH/1933229,1	

EXHIBIT C

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT C U.S. Patent No. 4,624,737

CI AIM TERMS	AGREED CONSTRUCTION
"eurface passivation film"	A thickness of material that provides protection such as
salitace passivances	electrical stability and chemical isolation.
"insulating substrate"	The material (such as glass, quartz, ceramic,
	insulator-coated silicon or insulator-coated metal) upon
	which the transistor is fabricated to provide mechanical
	support and electrical insulation.
"on said gate electrode and	Above and supported by or in contact with the gate
substrate"	electrode and the insulating substrate.
"them"	The gate insulating film, the high-resistivity semiconductor
	film, and the conducting film containing at least the low-
	resistivity semiconductor film.

EXHIBIT D

EXHIBIT D

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D U.S. Patent No. 4,624,737

		_				<u>)</u>											_	j				_	_	
Defendants' Support	Intrinsic Evidence:	'737 Patent, col. 1	lines 6-14; col. 2 line	61 – col. 2 line 2; col.	2 lines 8-10; col. 3	lines 22-24.		Extrinsic Evidence:	"Thin film	technology" for	circuits and systems is	defined as "a	technology in which a	thin film (a few	hundred to a few	thousand angstroms in	thickness) is applied	by vacuum deposition	to an insulating	substrate." IEEE	Standard Extrinsic	Evidence of Electrical	and Electronic Terms	939 (3rd ed. 1984)
Defendants' Construction	A semiconductor	device in which the	current flow between	source electrode and	drain electrode is	controlled by an	electric field that	penetrates the	semiconductor; this	field is introduced by	a voltage applied at	the gate electrode,	which is separated	from the	semiconductor by an	insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate.	,			
LPL's Support	Intrinsic Evidence:	'737 Patent at col. 1,	lines 6-29, 56-58, 61-	68; col. 2, lines 1-2, 8-	68; col. 3, lines 1-62;	col. 4, lines 1-23;	Figs. 1a-3d; and	claims 1-4. (LPL Exh.	1).		'737 patent discloses	various techniques for	fabricating thin films,	such as chemical	vapor deposition	(CVD) (e.g., 2:24-33),	sputtering (2:33-36),	molecular beam	deposition (4:19-20),	ion beam deposition	(4:19-20).		"Any suitable means	of applying the
LPL's Construction	A three-terminal	semiconductor device	in which the current	flow through one pair	of terminals, the	source and drain, is	controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	a voltage applied at	the third terminal, the	gate, which is	separated from the		insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate	rather than in a single	crystal silicon wafer.
Claim Term	thin-film transistor																							

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737		
U.S. Patent No. 4,624,7	3.7	
U.S. Patent No. 4	1,674,7	
U.S. Patent	No. 4	
	Patent	
	.v.	

Case 1:06-cv-00726-JJF

Defendants' Defendants' Support Construction	("1984 IEEE"), Exh.	<u>1</u> .	•	"A thin-film	transistor, TFT,	fabricated by	evaporation of all	components on to an	insulating substrate	has been developed"	Paul K. Weimer, The	TFT – A New Thin-	Film Transistor in 49	Proceedings of the	IRE 1462-64 (1962),	Exh. 2.							
LPL's Support C	various films	throughout this	procedure in the	vacuum may be	employed such as, for	example, evaporation,	sputtering, and the	like."	USPN 4,331,758 to	Luo issued May 25,	1982, col. 4, lines 11-	14 (LPL Exh. 2).		"A thin-film transistor	(TFT) is an insulated	grid field effect	transistor. It is similar	to a MOS transistor	(metal-oxide	semiconductor) with	the difference that it is	produced on an	amorphous substrate
LPL's Construction																							
Claim Term				-											-					-			

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT D

U.S. Patent No. 4,624,737

Defendants' Support														-									
Defendants' Construction												-										·	
LPL's Support	monocrystalline	silicon wafer. As they	are not limited by the	size of the crystalline	substrate, TFT circuits	can have very large	dimensions. The TFT	on an insulating	substrate has been	investigated in three	different ways"	USPN 4,426,407 to	Morin et al. issued	Jan. 17, 1984, col. 1,	lines 13-22 (emphasis	added) (LPL Exh. 3).	Extrinsic Evidence:	The Penguin	Dictionary of	Electronics 569 (3rd.	ed. 1998) ("1998	Penguin") ("thin-film	transistor (TFT) A
LPL's Construction																							
Claim Term					,																		

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D
U.S. Patent No. 4,624,737

Defendants' Support																								
Defendants' Construction																						٠.		
LPL's Support	MOSFET that is	fabricated using thin-	film techniques on an	insulating substrate	rather than on a	semiconductor chip.")	(LPL Exh. 4); id. at	205-207 ("field-effect	transistor (FET) It	is a three terminal	semiconductor device	in which the current	flow through one pair	of terminals, the	source and the drain,	is controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	the voltage applied at	the third terminal, the	gate"); id. at 70
LPL's Construction																								
Claim Term																								

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		("chip A small		
		piece of single crystal		
		of semiconductor		
		material containing		
		either a single		
		component or device		·
		or an integrated		
		circuit.").		
		See also The Penguin		
		Dictionary of		
		Electronics, 71, 186-		
		192, 583 (2nd. ed.		
		1988) ("1988		
	· .	Penguin") (LPL Exh.		
		5).		
gate electrode	A patterned,	Intrinsic Evidence:	A conductive element	Intrinsic Evidence:
	electrically conductive	"FIG. 2a shows in a	of a single thin-film	"Metals such as Cr,
	material that controls	sectional view the	transistor that controls	Mo, W, Al, Ta, etc.,
	current flow through	initial step for	the current between	and their silicides,
	the channel between	selectively forming a	source and drain by a	impurity-doped
	the source electrode	gate electrode 2 on an	voltage applied to its	polysilicon and other
	and drain electrode.	insulating substrate 1.	terminal. The gate	like materials can be

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D U.S. Patent No. 4,624,737

Defendants' Support	used as said gate	Patent, col. 2 lines 14-	16.	"FIG. 3a illustrates a	step in which gate	electrode 2 extending	along one line and	gate electrodes 2' on	another line are	formed on a	transparent insulating	substrate 1 such as	glass substrate." '737	Patent, col. 3 lines 26-	28. See also Figs. 1-3; 1	Col. 1 lines 15-17;		Extrinsic Evidence:	"Gate" is defined as a	structural element of a	TFT that "controls the	current between
Defendants' Construction		the gate pad associated P	ate	electrode.	S	<u>•</u>	<u></u>	8	<u>a</u>		T T	Ó		<u> </u>	2	O		<u> </u>	'	15		<u> </u>
LPL's Support	Metals such as Cr,	and their silicides,	impurity-doped	polysilicon and omer like materials can be	used as said gate	electrode 2." '737	Patent at col. 2, lines	7-16.		"FIG. 3a illustrates a	step in which gate	electrode 2 extending	along one line and	gate electrodes 2' on	another line are	formed on a	transparent substrate 1	such as a glass	substrate," '737	Patent at col. 3, lines	22-29.	
LPL's Construction																	. ,	-				
Claim Term																						

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
	·	See also Figs. 1-3; and claim 1.		source and drain by a voltage applied to its terminal." 1984 IEEE 384, Exh. 1.
	·			U.S. Patent No. 4,331,758 to Luo,
,				Figures 8 and 8A, col. 7 line 17 to col. 8 line 9, Exh. 15.
				"Gate" is defined as "[a]n electrode or electrodes in a field- effect transistor." See The Penguin
				Electronics, 237 (2nd. ed. 1988) ("1988 Penguin"), Exh. 18.
continuously depositing	The formation of the gate insulating film, the high-resistivity	Intrinsic Evidence: "[A]s shown in FIG. 1b, a gate insulating	Successively depositing each constituent film on top	Intrinsic Evidence: "[A] gate insulating film 3, a high-

U)						_
Defendants' Support	resistivity film 4, a	low-resistivity a-Si:H	(usually hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode	2 and substrate 1	without exposing them	to an oxidizing	atmosphere. Such	successive deposition	can be accomplished,	for instance, by	forming [films 3, 4	and 20] in the same	evacuated chamber in	a plasma CVD	apparatus. It is also	possible to form said	films successively in
Defendants' Construction	of the underlying film	or structure without	interruption and	without performing	any processing steps	between the	deposition of each	constituent film.					•											
LPL's Support	film 3 (such as silicon	nitride film) and an	amorphous silicon	film 4 are	continuously	deposited" '737	Patent at col. 1, lines	17-21.	-	"In the next step	illustrated in FIG. 2b	in a sectional view, a	gate insulating film 3,	a high-resistivity film	4, a low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode
LPL's Construction	semiconductor film	and conducting film	without intervening	films.																				
Claim Term															-									

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		2 and substrate 1		the respective
		without exposing them		chambers by using a
	- N C.	to an oxidizing		plasma CVD
		atmosphere. Such		apparatus having in-
		successive deposition		line chambers.
		can be accomplished,		Further, when a
		for instance, by		sputtering or
		forming [films 3, 4,		metalizing chamber is
		and 20] in the same		additionally provided,
		evacuated chamber in		conducting film 30
		a plasma CVD		can be also deposited
		apparatus. It is also		continuously without
		possible to form said		exposure to the
		films successively in		atmosphere." '737
		the respective		Patent, col. 2 lines 17-
		chambers by using a		36.
		plasma CVD		
		apparatus having in-		See also '737 Patent
:		line chambers.		Col. 1 lines 17-21, 32-
		Further, when a		54; col. 3 lines 28-35,
		sputtering or		53-62; col. 4 lines 1-
		metalizing chamber is		13; Abstract.
		additionally provided,		
		conducting film 30		Extrinsic Evidence:

						<u>)</u>											_)						
Defendants' Support	"Continuous" is	defined as "marked by	uninterrupted	extension in space,	time, or sequence."	1981 Webster's 243-	44, Exh. 3.	٠.	"Continuous" is	defined as "extending	or prolonged without	interruption or	cessation; unceasing,"	The American	Heritage Dictionary	317 (2d College Ed.	1985), Exh. 16.		W.E. Spear & P.G.	LeComber.,	Fundamental and	Applied Work on	Glow Discharge	Material, in The
Defendants' Construction																								
LPL's Support	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent at col 2, lines	17-37. See also '737	Patent at col. 3, lines	28-35, 54-62; col. 4,	lines 1-13; Abstract;	Figs. 2b and 3b; and	claims 1 and 2.		Extrinsic Evidence:	The American	Heritage College	Dictionary 1215 (2d	College Ed. 1985)	("1985 American	Heritage Dictionary")	(defining "successive"	as "[f]ollowing in an	uninterrupted order or	sequence.") (LPL Exh.	6); id. at 317 (defining
LPL's Construction																								
Claim Term											,													

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		"continuous" as		Physics of
		"extending or		Hydrogenated
		prolonged without		Amorphous Silicon I,
		interruption or		Chapter 3 64-68 (J.D.
		cessation;		Joannopoulos and G.
		unceasing").		Lucovsky eds.,
				Springer-Verlag 1984)
		The American		("1984 Spear")
		Heritage College		(describing vacuum
		Dictionary 301 (3d		deposition systems),
		College Ed. 1997)		Exh. 4.
		(defining "continuous"		
		as "uninterrupted in		P.G. LeComber &
		time, sequence,	-	W.E. Spear, The
		substance, or extent")		Development of the a-
		(LPL Exh. 7).		Si:H Field Effect
				Transistor and its
		1981 Webster's 243-		Possible Applications, 1-
		44 (defining		in 21D
		"[c]ontinuous" as		Semiconductors and
		"marked by		Semimetals 89-95
		uninterrupted		(1984) ("1984
		extension in space,		LeComber")
		time, or sequence.")		(describing single and
				, , , , , , , , , , , , , , , , , , ,

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		(Defendant's Exh. 3.)		multi-chamber
				deposition systems).
				Exh. 5.
•	•			T. Kodama et al., A
				Self-Alignment
				Process for
		•		Amorphous Silicon
				Thin Film Transistors,
				3-7 IEEE Electron
	-			Device Letters 187-89
				(Jul. 1982) ("1982
		-		Kodama") (describing
				a continuous
				deposition process).
		·		Exh. 6.
				Japanese patent
				publication JP 56-
				135968 to Osada et al.
				published October 23,
				1981, Figs. 1, 2; Cols.
				7-31 (describing
				continuous deposition

)											_	<u>) </u>						
Defendants' Support	of layers). Exh. 7.	TI DITTER	U.S. Fatent No.	1, Lines 9-54, Exh. 15.	Intrinsic Evidence:	'737 Patent, Figs. 1-3;	Col. 1 lines 17-21; col.	2 lines 17-32, 36-38;	col. 3 lines 28-35.	,	Extrinsic Evidence:	"Film" is defined as "a	thin covering or	coating" and "an	exceedingly thin	layer." 1981	Webster's 425, Exh. 3.	1	"Gate" is defined as a	structural element of a	TFT that "controls the	current between	source and drain by a
Defendants' Construction					A thickness of	material (such as	SiNx) that has high	electrical resistance	and insulates the gate	electrode from the	transistor	semiconductor.											
LPL's Support					Intrinsic Evidence:	"Such successive	deposition can be	accomplished, for	instance, by forming a	silicon nitride (SiNx)	film as gate insulating	film 3 from a mixed	gas of SiH ₄ and NH ₃ ,.	'737 Patent at	col. 2, lines 24-26.		"[A] multi-layer film.	. can be used as said	gate insulating film	3" '737 Patent at col.	2. lines 36-38.		See also '737 Patent at
LPL's Construction					A thickness of	material (such as	SiNx) that has high	electrical resistance	and insulates the	transistor gate from at	least the transistor	semiconductor.											
Claim Term					anto inculoting film	gate mountaining min													-1 i			·	

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		1:12-21, 2:18-38, 3:28-35: Abstract:	Collisti detion	
		1:12-21, 2:18-38, 3-28-35: Ahstract:		
		3-28-35: Abstract:		voltage applied to its
		りょし リフェ・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・		terminal." 1984 IEEE
		Figs 14-1d 2h-2e		384. Exh. 1.
		1153. 10-14, 20 20,		
		and 3b-3d; and claim		
		1.		"Insulating material"
				is defined as "a
		Extrinsic Evidence:		substance or body, the
		1988 Penguin at 194		conductivity or which
		(defining "film" as a		is zero or, in practice,
		"coating with a		very small." 1984
		minimal thickness		IEEE 447, Exh. 1.
		dimension.") (LPL		
		Fxh. 5).		"Layer" is defined as a
				"thickness, coating, or
		1985 American		stratum spread out or
-		Heritage Dictionary at	,	covering a surface."
		710 / J. E		1085 Amorican
	•	/19 (denning layer		190) American
		as a "thickness,		Heritage Dictionary
		coating, or stratum		719, LPL Exh. 6.
		spread out or covering		
		a surface.") (LPL Ex.		
		6).		
high-resistivity A thickness of	ness of	Intrinsic Evidence:	A thickness of	Intrinsic Evidence:
semiconductor film semiconductor	nductor	"Such successive	semiconductor with no	"Such successive

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737

			•,)																		
Defendants' Support	deposition can be	accomplished, for	instance, by	forming a high-	resistivity a-Si:H film	4 by using SiH ₄ in	the same evacuated	chamber in a plasma	CVD apparatus."	'737 Patent, col. 2	lines 23-29.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,	for instance, SiF4, or a	microcrystalline	amorphous silicon
Defendants' Construction	intentionally added	impurities to increase	its conductivity,	resulting in an	electrical resistance	many orders of	magnitude higher than	a low-resistivity	semiconductor film.															
LPL's Support	deposition can be	accomplished, for	instance, by	forming a high-	resistivity a-Si:H film	4 by using SiH ₄ and	forming a n ⁺ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4	in the same evacuated	chamber in a plasma	CVD apparatus."	'737 patent at col. 2,	lines 23-29.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,
LPL's Construction	material (such as	amorphous silicon,	hydrogenated	amorphous silicon,	amorphous silicon-	fluorine alloy,	amorphous silicon-	hydrogen-fluorine	alloy, or a	microcrystalline	amorphous silicon)	that has a higher	resistance to current	flow relative to the	low-resistivity	semiconductor film	(later recited in the	claim).						
Claim Term																								

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

Claim Term	I pr. Construction	T DI 3. Ch		
		LFL's Support	Construction	Detendants' Support
		for instance, SiF4, or a		film." '737 Patent,
		microcrystalline		col. 2 lines 38-43.
,		amorphous silicon		
		film." '737 patent at		See also '737 Patent,
		col. 2, lines 38-43.		Figs. 1-3; col. 1 lines
				8-11, 17-32; col. 2
		See also '737 Patent at		lines 17-32; col. 3
		col. 1, lines 8-29, 32-		lines 28-35.
		46, col. 2, lines 17-32,		
		38-43, 54-60; col. 3,		Extrinsic Evidence:
		lines 7-10, 16-21, 28-		Shyh Wang, Solid
-		41, 48-62; col. 4, lines		State Electronics 129,
		1-23; Abstract; Figs.		155 (McGraw Hill
		1b-1d, 2b-2e, and 3b-		1966) ("1966 Wang")
	-	3d; and claims 1 and		(describing relative
		2.		properties of
				conductors,
		Extrinsic Evidence:		semiconductors and
		1988 Penguin at 131		insulators), Exh. 8
		(defining "doping		
		level" as a "[t]he		P.G. LeComber,
		amount of doping		Doping and the
		necessary to achieve		Density of States of
		the desired		Amorphous Silicon, in

Defendants' Support	Fundamental Physics	of Amorphous	Semiconductors 46-55	(F. Yonezawa ed.,	Springer-Verlag 1981)	("1981 LeComber")	(comparing doped and	nndoped	semiconductors), Exh.	9.		1984 Spear 91-97	(comparing doped and	nudoped	semiconductors), Exh.	4.	See also 1984	LeComber 89-95, Exh.	5; K.D. MacKenzie et	al., The	Characteristics and	Properties of	Optimised Amorphous
Defendants' Construction																							
LPL's Support	characteristic in a	semiconductor. Low	doping levels give	a high-resistivity	material; high doping	levels give a low-	resistivity material.")	(LPL Exh. 5).		Id. at 194 (defining	"film" as a "coating	with a minimal	thickness dimension.")										
LPL's Construction																							
Claim Term																							

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Coust action	
				Silicon Field Effect
				Transistors, in A31
				Applied Physics A,
				Solids and Surfaces
				87-88 (1983) ("1983
				MacKenzie"). Exh.
				10.
		_		
				"Layer" is defined as a
				"thickness, coating, or
				stratum spread out or
				covering a surface."
				1985 American
				Heritage Dictionary
				719, LPL Exh. 6.
conducting film	A thickness of	Intrinsic Evidence:	A thickness which	Intrinsic Evidence:
	electrically conductive	Claim 1 of the '737	includes a material	"[A] conducting film
	maternal.	patent, which recites	consisting of an	30 made of a metal or
		"a conducting film	elemental metal, metal	other material" '737
		containing at least a	alloy, or film of	Patent, Col. 2 lines 17-
		low-resistivity	optically transparent	23.
		semiconductor film."	material, and having	
			an electrical resistance	"Further, when a
		Claim 2 of the '737	several orders of	sputtering or

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))			سنيب			
Defendants' Support	metalizing chamber is	additionally provided,	conducting film 30	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent, col. 2 lines 32-	36.		"As said conducting	film 30, it is desirable	to use a stable	conducting film such	as a transparent	conducting film made	of a refractory metal	such as Cr, W, Mo,	Ta, etc., and silicides	thereof, or indium-tin-	oxide (ITO), SnO ₂ and	the like. Use of a	transparent conducting	film has the advantage
Defendants' Construction	magnitude lower than	a low-resistivity	semiconductor film.								-													
LPL's Support	patent, which recites	"said conducting film	is composed of at least	two layers consisting	of a low-resistivity	semiconductor film	and thereon a	refractory metal film	or transparent	conducting film."		"In this example, no	conducting film is	formed on low-	resistivity amorphous	silicon film 20, but a	conducting film such	as ITO film may be	formed on said low-	resistivity film 20 as	in the example shown	in FIG. 2." '737	patent at col. 3, lines	48-52.
LPL's Construction																								
Claim Term																								 !

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				that the process is
		"In the next step		simplified when the
		illustrated in FIG. 2b		thin-film transistor of
		in a sectional view, a		this invention is
,		gate insulating film 3,		applied to an active
		a high-resistivity film		matrix liquid crystal
		4, a low-resistivity a-		display." '737 Patent,
		Si:H (usually		col. 2 lines 46-53.
		hydrogenated		
		amorphous silicon)		"The same materials
		film 20 and a		as used for conducting
		conducting film 30		film 30 and other
		made of a metal or		materials such as Al
		other material are		can be used for said
		successively formed		drain and source
		on said gate electrode	-	electrode members 15,
		2 and substrate 1"		16." '737 Patent, col.
		'737 patent at col. 2,		3 lines 4-7.
		lines 17-23.		
				"In this example, no
		"As said conducting		conducting film is
		film 30, it is desirable		formed on low-
		to use a stable		resistivity amorphous
		conducting film such		silicon film 20, but a

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		as a transparent		conducting film such
		conducting film made		as ITO film may be
		of a refractory metal		formed on said low-
		such as Cr, W, Mo,		resistivity film 20 as
		Ta, etc., and silicides		in the example shown
		thereof, or indium-tin-		in FIG. 2." '737
		oxide (ITO), SnO ₂ and		Patent, col. 3 lines 48-
		the like." '737 patent		52.
		at col. 2, lines 46-50.		
				"The same is true with
		See also '737 Patent at		the interface of low-
		col. 1, lines 25-29, 32-		resistivity amorphous
		51, col. 2, lines 10-36,		silicon film 20 and
•		43-68; col. 3, lines 1-		conducting film 30.
		10, 28-35, 48-62; col.		Further, since the
		4, lines 1-23; Abstract;		interfaces of low-
		Figs. 2b-2e and 3b-3d.		resistivity amorphous
				silicon film 20 or
		"Deposition of a		conducting film 30
		metallic grid coating		and drain and source
		24, e.g. of highly		electrodes 15, 16 can
		doped silicon or		be cleaned" '737
		aluminum (by CVD-		Patent, col. 3 line 57 –
		plasma) on the entire		col. 4 line 2.

Defendants' Support	See also '737 Patent,	Figs. 1-3; col. 2 lines 54-60.	Extrinsic Evidence: "Electrically	conductive materials	that can be prepared	by CVD comprise	elemental metals,	metal alloys,	superconductive	compounds, and films	of optically	transparent	conductors." Thin	Film Processes 315-	317 (J.L. Vossen &	W. Kern eds.,	Academic Press 1978,	Exh. 11.	
Defendants'	HOHON HETIOO																		
LPL's Support	surface of the sample(g)." USPN	4,420,407 to Monn et al. issued Jan. 17, 1984, col. 3, lines 50-	52 (LPL Exh. 3).	" wherein the	conductive coating is	of highly doped	silicon and is obtained	by reactive gaseous	phase plasma." Id. at	claims 5. See also id.	at claims 1, 3, and 4.		Extrinsic Evidence:	1985 American	Heritage Dictionary at	307 (defining	"conduct[ing]" as	"serv[ing] as a	medium or channel for l
LPL's Construction																			
Claim Term							,				•								 .

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Defendants' Support	129, 155, Exh. 8; 1984 Spear 91-97, Exh. 4.	See also support cited	by LPL for the term "conducting film".																
Defendants' Construction																			
LPL's Support	6).	1988 Penguin at 194 (defining "film" as a	"coating with a minimal thickness	dimension.") (LPL	Exh. 5).	CRC Handbook of	Chemistry and Physics	12-96 (75th ed., 1994-	1995) (discussing the	resistivity of	semiconducting	minerals) (LPL Exh.	9).	Thin Film Processes	316-317 (J.L. Vossen	& W. Kern eds.,	Academic Press 1978,	(noting that "[t]hin	films of optically
LPL's Construction																-			
Claim Term																			

)											<u>)</u>	_					
Defendants' Support		Intrinsic Evidence:	"[A] low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 are	successively formed	Such successive	deposition can be	accomplished, for	instance, by	forming a n+ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4 in	the same evacuated	chamber in a plasma	CVD apparatus"
Defendants' Construction		A thickness of	semiconductor having	intentionally added	impurities to increase	its conductivity,	resulting in an	electrical resistance	many orders of	magnitude lower than	a high-resistivity	semiconductor film.						
LPL's Support	transparent and electrically conductive materials", including SnO ₂ , are "usually classified" as semiconductors) (Defendants' Exh. 11).	Intrinsic Evidence:	"In the next step	illustrated in FIG. 2b	in a sectional view, a	gate insulating film 3,	a high-resistivity film	4, a low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	on said gate electrode	2 and substrate 1
LPL's Construction		A thickness of	semiconductor	material (such as low-	resistivity amorphous	silicon, hydrogenated	amorphous silicon,	amorphous silicon-	fluorine alloy,	amorphous silicon-	hydrogen-fluorine	alloy, or a	microcrystalline	amorphous silicon,	which contains	phosphorous or other	impurities to enhance	the conductivity of the
Claim Term		low-resistivity	semiconductor film		,													

J		7						<u>) </u>	<u>-</u>										-	<u> </u>						
	Defendants' Support		'737 Patent, col. 2	lines 17-32.		"Such alloys [a-Si:F	or a-Si:H:F alloy	using, for instance,	SiF ₄ , or a	microcrystalline	amorphous silicon	film] can be also used	for said low-resistivity	amorphous silicon	film 20, and such film	may contain other	impurites beside	phosphorous	impurities." '737	Patent, col. 2 lines 38-	45.		"In this example, no	conducting film is	formed on low-	resistivity amorphous
	Defendants'	Construction														-										
	LPL's Support	:	without exposing them	to an oxidizing	atmosphere. Such	successive deposition	can be accomplished,	for instance, by	forming a n ⁺ a-Si:H	film 20 from a mixed	gas of PH3 and SiH4	.," '737 patent at col.	2, lines 17-30.		"In place of said high-	resistivity amorphous	silicon film 4, there	can be used a film of	amorphous silicon-	fluorine alloy (a-Si:F)	or amorphous silicon-	hydrogen-fluorine	alloy (a-Si:H:F) using,	for instance, SiF4, or a	microcrystalline	amorphone eilicon
1.34.1.2	LPL's Construction		film) that has a lower	resistance to current	flow relative to the	high-resistivity	semiconductor film.													·						
	Claim Term																	-								

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
		film. Such alloys can		silicon film 20, but a
		be also used for said		conducting film such
		low-resistivity		as ITO film may be
		amorphous silicon		formed on said low-
		film 20, and such film		resistivity film 20 as
		may contain other		in the example shown
		impurities beside		in FIG. 2." '737
		phosphorous		Patent, col. 3 lines 48-
		impurities." '737		52.
		patent at col. 2, lines		
		38-50.		"The same is true with
				the interface of low-
		See also '737 Patent at		resistivity amorphous
		col. 1, lines 25-29,		silicon film 20 and
		32-51; col. 2, lines 17-		conducting film 30.
		45, 54-68; col. 3, lines		Further, since the
		1-10, 28-41, 48-62;		interfaces of low-
		col. 5, lines 1-23;		resistivity amorphous
		Abstract; Figs. 1d; 2b-		silicon film 20 or
		2e, and 3b-3d; and		conducting film 30
		claims 1 and 2.		and drain and source
				electrodes 15, 16 can
		Extrinsic Evidence:		be cleaned" '737
		1988 Penguin at 131		Patent, col. 3 line 57 –

						_	i			•								_)		_				
Defendants' Support		col. 4 line 2.		See also '737 Patent,	Figs. 1-3; Col. 1 lines	8-11, 17-32; col. 2	lines 32-36, 46-60;	col. 3 lines 4-7.		Extrinsic Evidence:	1984 Spear 91-97.	Exh. 4; 1984	LeComber 89-95, Exh.	5; 1966 Wang 129,	155, Exh. 8; 1981	LeComber 46-55, Exh.	9; 1983 MacKenzie	87-88. Exh. 10.		"Layer" is defined as a	"thickness, coating, or	stratum spread out or	covering a surface."	1985 American	Heritage Dictionary
Defendants'	Construction							-																	
LPL's Support		(defining "doping	level" as a "[t]he	amount of doping	necessary to achieve	the desired	characteristic in a	semiconductor. Low	doping levels give	a high-resistivity	material; high doping	levels give a low-	resistivity material.")	(LPL Exh. 5).		Id. at 194 (defining	"film" as a "coating	with a minimal	thickness	dimension.").					
LPL's Construction		-																				1.118			
Claim Term																									

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Defendants' Support	719, LPL Exh. 6.	Intrinsic Evidence:	"[A] low-resistivity a-	Si:H (usually	hydrogenated	amorphous silicon)	film 20 and a	conducting film 30	made of a metal or	other material are	successively formed	". '737 Patent, col.	2 lines 17-23.	"In this example, no	conducting film is	formed on low-	resistivity amorphous	silicon film 20, but a	conducting film such	as ITO film may be	formed on said low-	resistivity film 20 as	in the example shown
Defendants' Construction		A conducting film	with an adjoining thin	layer of low-resistivity	semiconductor and	possibly other	adjoining layers.																
LPL's Support		Intrinsic Evidence:	Claim 2 of the '737	patent, which recites	"said conducting film	is composed of at least	two layers consisting	of a low-resistivity	semiconductor film	and thereon a	refractory metal film	or transparent	conducting film."	Compare '737 patent	at col. 3, lines 40-	41("exposed portion	of low-resisitivity	amorphous silicon	film 20 is removed"),	Figs. 2d and 3c with	Claim 1 ("a fifth step	for selectively	removing said
LPL's Construction		The conducting film is	composed of a low-	resistivity	semiconductor film	and possibly other	conductive films.																
Claim Term		conducting film	containing at least a	low-resistivity	semiconductor film	-													•				

	,				<u>)</u>)						
Defendants' Support	in FIG. 2." '737	Patent, col. 3 lines 48-	52.	"The same is true with	the interface of low-	resistivity amorphous	silicon film 20 and	conducting film 30.	Further, since the	interfaces of low-	resistivity amorphous	silicon film 20 or	conducting film 30	and drain and source	electrodes 15, 16 can	be cleaned". '737	Patent, col. 3 line 57 –	col. 4 line 2.		"A gate insulating	film, a high-resistivity	semiconductor film, a	low-resistivity
Defendants' Construction				,																	-		
LPL's Support	conducting film	exposed on said island	region").	Claim 1 ("a third step	in which said high	resistivity	semiconductor film	and said conducting	film are selectively	etched") (note no	separate mention is	made of low	resistivity	semiconductor film).		See also '737 patent at	col. 1, lines 18-36, 43-	57; col. 3, lines 28-41,	48-62; col. 4, lines 1-	12; Figs 2b-2e, 3b-3d;	claim I.	· · · · ·	" wherein the
LPL's Construction																							
Claim Term																							

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

LPL's Support conductive coating is
of highly doped silicon and is obtained
by reactive gaseous phase plasma." USPN
4,426,407 to Morin et
1984, claim 5 (LPL
Exh. 3). See also id.
col. 3, lines 50-52;
claims 1, 3, and 4.
Extrinsic Evidence:
1985 American
Heritage Dictionary at
315-316 (defining
"contain" as "to have
as component parts;
comprise; include")
(LPL Exh. 6).
1988 Penguin at 93
(defining "conductor"
as a "fal material that

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
		offers a low resistance		Webster's 576, Exh. 3.
		to the passage of		
		electrical current:		"Conducting material"
,		when a potential		is defined as "a
	-	difference is applied		conducting medium in
		across it a relatively		which the conduction
		large current flows.")		is by electrons, and
	-	(LPL Exh. 5).		whose temperature
				coefficient of
		<i>Id.</i> at 131 (defining		resistivity is, except
		"doping level" as a		for certain alloys,
		"[t]he amount of		nonnegative at all
		doping necessary to		temperatures below
		achieve the desired		the melting point."
		characteristic in a		1984 IEEE 175, Exh.
		semiconductor. Low		1.
		doping levels give		`
		a high-resistivity		"Semiconductor" is
		material; high doping		defined as "an
		levels give a low-		electronic conductor
		resistivity material.").		with resistivity in the
				range between metals
_				and insulators, in
				which the electric-

Defendants' Support	charge-carrier	concentration	increases with	increasing temperature	over some temperature	range". 1984 IEEE	815, Exh. 1.	See also 1983	MacKenzie 87-88.	Exh. 10; Japanese	patent publication JP	58-190061 to Aoki et	al. published	November 5, 1983,	Figs 4, 5; Cols. 7-9.	Exh. 12	"Layer" is defined as a	"thickness, coating, or	stratum spread out or	covering a surface."	1985 American	Heritage Dictionary
Defendants' Construction																						
LPL's Support																			1. 40			
LPL's Construction																						
Claim Term																						

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Tre s auppoin
Intrinsic Evidence:
"In the conventional
process shown in
FIGS. 1a to 1d, since
the masking step
precedes the
deposition of n+
amorphous films 25,
26, natural oxide is
produced on the
exposed surface of
amorphous silicon
film 4. Although such
natural oxide can be
removed by an
aqueous solution of
hydrofluoric acid (HF)
or a similar substance,
the possibility is still
great that oxygen and
its compounds as well
as other impurities can
collect on the laminate

Defendants' Support															,								
Defendants' Construction												-											
LPL's Support	surface as it is	exposed to the	atmosphere. This	would give rise to	electrical resistance	between the source	and drain and between	channels in the thin-	film transistor thus	obtained, making such	transistor unable to	exhibit its desired	characteristics." '737	patent at col. 1, lines	32-44.	"As described above,	according to the	present invention, no	oxides, etc., are	formed at the interface	of high-resistivity	amorphous silicon	film 4 and low-
LPL's Construction																							
Claim Term																						-	

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Defendants' Support																								
Defendants' Construction																								
LPL's Support	resistivity amorphous	silicon film 20, so that	a good junction can be	formed. The same is	true with the interface	of low-resistivity	amorphous silicon	film 20 and	conducting film 30.	Further, since the	interfaces of low-	resistivity amorphous	silicon film 20 or	conducting film 30	and drain and source	electrodes 15, 16 can	be cleaned without	damaging the high-	resistivity amorphous	silicon film, a good	contact can be	obtained without	sacrificing the	inherent properties of
LPL's Construction			•																					
Claim Term																								

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Defendants' Support				Intrinsic Evidence: "In the conventional	process shown in	FIGS. 1a to 1d, since the masking step	precedes the	deposition of n+	amorphous films 25,	26, natural oxide is	produced on the
Defendants' Construction				Without permitting the gate insulating film,	high-resistivity	semiconductor film, low-resistivity	semiconductor film, or	conducting film to	come into contact with	an atmosphere that	would create an oxide
LPL's Support	thin-film transistor." '737 patent at col. 3, line 53 – col. 4, line 2. See also '737 Patent at col. 1, lines 21-51; col. 2 lines 17-53; col. 3 lines 28-35 53-62.	col. 4, lines 1-23; Abstract; Figs 2b-2e, 3b-3d; and claims 1	and 2.	Intrinsic Evidence: '737 patent at col. 1,	lines 32-44, 47-53;	col. 2, lines 17-36; col. 3, lines 28-35, 53-	62; col. 4, lines 1-12;	Figs. 2b-2e, 3b-3d;	claims 1 and 2.	. *	
LPL's Construction				This phrase is a combination of	previously defined or	agreed constructions of "them" and	"oxidizing	atmosphere", namely,	the gate insulating	film, the high-	resistivity
Claim Term				without exposing them to an oxidizing	atmosphere						

Defendants' Support	exposed surface of	amorphous silicon	film 4. Although such	natural oxide can be	removed by an	aqueous solution of	hydrofluoric acid (HF)	or a similar substance,	the possibility is still	great that oxygen and	its compounds as well	as other impurities can	collect on the laminate	surface as it is	exposed to the	atmosphere. This	would give rise to	electrical resistance	between the source	and drain and between	channels in the thin-	film transistor thus	obtained, making such	transistor unable to
Defendants' Construction	on any of these four	films.																						
LPL's Support											,										-			
LPL's Construction	semiconductor film,	and the conducting	film containing at least	a low-resistivity	semiconductor film	are deposited without	exposure to an	atmosphere that would	create substantial	oxidation on any of	these films.						-					,		
Claim Term								•		•							-							

Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				exhibit its desired
				characteristics." '737
				Patent, col. 1, lines
				32-46.
				"[Films 3, 4, 20 and
	-			30] are successively
				formed on said gate
	-			electrode 2 and
				substrate 1 without
-				exposing them to an
			,	oxidizing atmosphere.
	,			Such successive
				deposition can be
				accomplished, for
				instance, by forming
				[films 3, 4 and 20] in
		,		the same evacuated
				chamber in a plasma
				CVD apparatus. It is
				also possible to form
				said films successively
				in the respective
	·			chambers by using a

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Defendants' Support	plasma CVD apparatus having in-	line chambers.	Further, when a	sputtering or	metalizing chamber is	additionally provided,	conducting film 30	can be also deposited	continuously without	exposure to the	atmosphere." '737	Patent, col. 2 lines 17-	36.	"As described above	according to the	present invention, no	oxides, etc., are	formed at the interface	of high-resistivity	amorphous silicon	film 4 and low-	resistivity amorphous
Defendants' Construction																						
LPL's Support																						
LPL's Construction																						
Claim Term										,											,	

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

Defendants' Support	silicon film 20, so that	a good junction can be	formed. The same is	true with the interface	of low-resistivity	amorphous silicon	film 20 and	conducting film 30."	'737 Patent, col. 3,	line 53-59.	"A gate insulating	film, a high-resistivity	semiconductor film, a	low-resistivity	semiconductor film	and if necessary a	conducting film are	successively deposited	in lamination without	exposing them to any	oxidizing atmosphere	including atmospheric	air," '737 Patent,
Defendants' Construction																	_					-	
LPL's Support										,													
LPL's Construction																				•			
Claim Term																							

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v				<u>)</u>											_	<u>)</u>						
Defendants' Support	Abstract.	Extrinsic Evidence:	1984 Spear 64-68, 91-	9/, EXh. 4; 1984	5; 1982 Kodama 187-	89. Exh. 6; Japanese	patent publication JP	56-135968 to Osada et	al. published October	23, 1981, Figs. 1, 2;	Cols. 7-31. Exh. 7.	Intrinsic Evidence:	"FIG. 2c illustrates the	step in which said	conducting film 30,	low-resistivity	amorphous silicon	film 20 and high-	resistivity amorphous	silicon film 4 are left	as an island region by	etching in a single
Defendants' Construction												Have a selected	portion of the	substance of the	conducting film, low-	resistivity	semiconductor film	and high-resistivity	semiconductor film	removed using an	etching technique.	
LPL's Support												Intrinsic Evidence:	"Fig. 2c illustrates the	step in which said	conducting film 30,	low-resistivity	amorphous silicon	film 20 and high-	resistivity amorphous	silicon film 4 are left	as an island region by	etching in a single
LPL's Construction		·		·								The removal of	selected portions of a	surface using etching	techniques (such as	wet etching, plasma	etching, reactive ion	etching, and ion	etching) in order to	produce a desired	pattern on the surface.	
Claim Term		,,							·			selectively etched										

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

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Defendants' Support	masking step. Known	etching techniques	such as wet etching,	plasma etching,	reactive ion etching,	ion etching, etc., can	be used for this step."	'737 Patent, col. 3	lines 54-60.		See also '737 Patent,	Figs. 1-3; Col. 1 lines	17-21, 25-29; col. 2	lines 60-66; col. 3	lines 7-10, 44-48.									
Defendants' Construction																								
LPL's Support	masking step. Known	etching techniques	such as wet etching,	plasma etching,	reactive ion etching,	etc., can be used for	this step." '737 patent	at col. 2, lines 54-60.		See also '737 Patent at	col. 1, lines 14-21, 25-	29, 32-35; col. 2, lines	10-16, 54-66; col. 3,	lines 7-10, 28-41, 44-	48; col. 4, lines 3-9;	Figs. 1a-1d; 2a-2e; 3a-	3e; and claim 1.		USPN 4,331,758 to	Luo issued May 25,	1982 (compare col. 7,	line 39 – col. 8, line	10 (describing a wet	etch) with col. 5, lines
LPL's Construction																		• ***						
Claim Term										·			,											

Defendants' Defendants' Support Construction		Defendants contend See support for claim
LPL's Support	1-27 (describing the use of a non-etching technique for forming a patterned surface)) (LPL Exh. 2). Extrinsic Evidence: "etching Chemical erosions of selected portions of a surface in order to produce a desired pattern on the surface." 1988 Penguin 170-71 (LPL Exh. 5). Cf. id. at 299-300 (defining "lift off"). USPN 4,404,731 to Poleshuk issued Sep. 20, 1983 (LPL Exh. 8).	<u>Intrinsic Evidence:</u> Defendants contend
LPL's Construction		A discrete portion of
Claim Term		island region

JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

U.S. Patent No. 4,624,737

, Defendants' Support	part on said gate and electrode" below.					
Defendants' Construction	be interpreted as part of the phrase "island region on said gate electrode."					
LPL's Support	step in which said conducting film 30, low-resistivity amorphous silicon	film 20 and high- resistivity amorphous silicon film 4 are left as an island region by	etching in a single masking step. Known etching techniques	such as wet etching, plasma etching, reactive ion etching,	ton etching, etc., can be used for this step." '737 patent at col. 2, lines 54-57.	See also '737 Patent at col. 2, lines 54-60; col. 3, lines 28-35; Figs. 2c-2e, 3c-3d; and
LPL's Construction	semiconductor film and conducting film that is formed by selective etching.					
Claim Term						

]											_	<u>)</u>					
Defendants' Support	Intrinsic Evidence: The '737 patent	drawings show an	island of material with	no other surrounding	material. '737 Patent,	Figs. 2c, 3b.		"FIG. 2c illustrates the	step in which said	conducting film 30,	low-resistivity	amorphous silicon	film 20 and high-	resistivity amorphous	silicon film 4 are left	as an island region by	etching in a single	masking step." '737	Patent, col. 2 lines 54-	57.	See also '737 Patent,	col. 3 lines 28-35.
Defendants' Construction	Portion of the conducting film, low-	resistivity	semiconductor film	and high-resistivity	semiconductor film	which has been etched	around its entire	perimeter into a	separate isolated	region located over the	gate electrode of a	single thin-film	transistor.									
LPL's Support	See definitions of "island region" and,	"gate electrode",	supra.																-			
LPL's Construction	This phrase is a combination of	previously defined or	agreed constructions	of "island region",	"on", and "gate	electrode", namely, a	discrete portion of the	high-resistivity	semiconductor film	and conducting film	that is formed by	selective etching. The	discrete portion is	located above and	supported by or in	contact with the gate	electrode.			-		
Claim Term	island region on said gate electrode)																				

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendants' Support
				Extrinsic Evidence:
				"Island" is defined as
				"1: a tract of land
				surrounded by water
				and smaller than a
· · ·				continent 2:
				something resembling
				an island esp. in its
· · · · ·				isolated or surrounded
·				position". 1981
				Webster's 608. Exh. 3.
				A.J. Snell et al.,
				Application of
			•	Amorphous Silicon
				Field Effect
-				Transistors in
				Addressable Liquid
				Crystal Display
	,			Panels, in 24 Applied
				Physics at 357, 358
				(April 1981), Exh. 17.
selectively forming	Forming a pattern of	Intrinsic Eyidence:	Forming in selected	Intrinsic Evidence:

							r								_							
Defendants' Support	'737 Patent, Figs. 1-3; Col. 1 lines 15-17; col.	2 lines 10-14, 60-66;	col. 3 lines 34-41;	Abstract.			Intrinsic Evidence:	'737 Patent, Figs. 1-3;	Col. 1 lines 15-17; col.	2 lines 10-14, 60-66;	col. 3 lines 4-7, 36-44;	Abstract.										
Defendants' Construction	regions only.						Forming a source	electrode and drain	electrode in selected	regions only by	depositing a	conducting film or	other material such as	AI.	-							
LPL's Support	'737 Patent at col. 1, lines 14-17, 25-29;	col. 2, lines 10-36, 60-	68; col. 3, lines 1-10,	24-52; col. 4, lines 3-	9; Abstract; Figs. 1a-	claim 1.	Intrinsic Evidence:	"In the next step	illustrated in FIG. 3c,	a transparent	conducting film such	as ITO film is	deposited; then, drain	electrode 15 and	source electrode 16	which doubles as a	picture cell electrode	are selectively formed	and the exposed	portion of low-	resistivity amorphous	silicon film 20 is
LPL's Construction	material (for example, by depositing material	and selectively etching	portions of the	material away).			The source electrode	and drain electrode are	selectively formed	together.												
Claim Term							a fourth step for	selectively forming a	source electrode and	drain electrode							•					

Defendants' Support		Intrinsic Evidence: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to form drain and source electrodes 5, 6, thereby completing a thin-film transistor unit." '737 Patent,
Defendants' Construction		A conductive element of a single thin-film transistor formed over the source region from which charge carriers flow into the channel toward the drain. The source electrode is distinct from the source/data line and the source/data pad associated with the source electrode.
LPL's Support	removed." '737 Patent at col. 3, lines 36-41. See also '737 Patent at col. 1, lines 21-29, 32-51; col. 2, lines 17-68; col. 3, lines 1-14, 28-62; col. 4, lines 1-12; Abstract; Figs. 1d, 2d-2e, 3c-3d; and claim 1.	"Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15,
LPL's Construction		A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
Claim Term		source electrode

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
		16 serving at least as a		col. 1 lines 25-29.
		part of the mask"		
		,737 Patent at col. 2,		See also '737 Patent,
		lines 60-66.		Figs 1d, 2d-2e, 3c-3d;
•	-			Col. 2 lines 60-66; col.
		"In the final step		3 lines 36-41, 57-62.
		illustrated in FIG. 2e,		
		a surface passivation		Extrinsic Evidence:
		film 8 is deposited,		"Source" is defined as
,		and the drain and		a device structure
		source electrodes 15,	•	which "contains the
		16 and gate electrode		terminal from which
		2 are partly exposed		charge carriers flow
		(not shown)." '737		into the channel
		Patent at col. 3, lines		toward the drain. It
		11-14.		has the potential
				which is less attractive
		See also '737 Patent at		than the drain for the
		col. 1, lines 21-29, 32-		carriers in the
		51; col. 2, lines 17-68;		channel." 1984 IEEE
		col. 3, lines 1-14, 28-		855, Exh. 1.
		62; col. 4, lines 1-12;		
		Abstract; Figs. 1d, 2d-		"Source" is defined as
		2e, 3c-3d; and claim 1.		"[t]he electrode in a

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT D

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Defendants' Support	field-effect transistor	that supplies charge	carriers (holes or	electrons) to the	interelectrode space."	1998 Penguin 532,	Exh. 18.																	
Defendants' Construction																								
LPL's Support		"[A]II of the source	electrodes 23 in any	column are electrically	connected together	since each source	electrode forms a	portion of the source	bus conductor. By	electrically addressing	any given column	source bus conductor	23 and any given row	gate bus conductor, a	single transistor of the	array can be turned on,	thereby permitting	current to flow from	its source through the	conductive channel of	the semiconductive	material to the	corresponding drain.	This then can be
LPL's Construction																			,					
Claim Term															-									

	/	
Defendants' Support		Intrinsic Evidence: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and selectively etched to
Defendants' Construction		A conductive element of a single thin-film transistor formed over the drain region into which charge carriers flow from the source into the channel.
LPL's Support	utilized to alter the field across an electrooptical device, such as a liquid crystal layer, thus providing an optical read-out of a bit of information." USPN 4,331,758 to Luo issued May 25, 1982 at col. 7, lines 40-58; col. 8, lines 1-10 (LPL Exh. 2). See also id. Figs. 8 and 8A.	"Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30
LPL's Construction		A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode
Claim Term		drain electrode

Defendants' Support	form drain and source	electrodes 5, 6,	thereby completing a	thin-film transistor	unit." '737 Patent,	col. 1 lines 25-29.		See also '737 Patent,	Figs 1d, 2d-2e, 3c-3d;	Col. 2 lines 60-66; col.	3 lines 36-41, 57-62.		Extrinsic Evidence:	"Drain" is defined as a	device structure which	"contains the terminal	into which charge	carriers flow from the	source into the	channel. It has the	potential which is	more attractive than	the source for the	carriers in the
Defendants' Construction																						-		
LPL's Support	amorphous silicon	film 20 shown in FIG.	2c are selectively	removed with said	electrode members 15,	16 serving at least as a	part of the mask "	² 737 Patent at col. 2,	lines 60-66. See also	'737 Patent at col. 1,	lines 21-29, 32-51;	col. 2, lines 17-68;	col. 3, lines 1-14, 28-	62; col. 4, lines 1-12;	Abstract; Figs. 1d, 2d-	2e, 3c-3d; and claim 1.				,				•
LPL's Construction	gate electrode.								,														-	
Claim Term																								

Defendants' Support	channel." <i>1984 IEEE</i> 276, Exh. 1.	"Drain" is defined as "[t]he electrode of a field-effect transistor through which carriers leave the interelectrode space." 1998 Penguin 152, Exh. 18.	Intrinsic Evidence: '737 Patent, Figs. 1d, 2d-2e, 3c-3d; Col. 1 lines 25-29; col. 2 lines 60-66; col. 3 lines 36-41, 57-62. Extrinsic Evidence: The verb "contact" is defined as "to bring into contact with" and the noun is defined as
Defendants' De- Construction		"Dr. "[t]] field thro leav inter 1999	Touching a part of the Surface of the island 2d-2 lines line
LPL's Support			Intrinsic Evidence: Su '737 Patent at col. 3, re, lines 53-62, col. 4, lines 1-2; Figs. 2d-2e; 3c-3d. Extrinsic Evidence: 1985 American Heritage Dictionary at 315 (defining "contact" as a
LPL's Construction			Forming an electrical connection to a part of the surface of the island region.
Claim Term			contacting a part of the surface of said island region

	<u> </u>		
Defendants' Support	"a union or junction of surfaces" or "the junction of two electrical conductors through which a current passes." 1981 Webster's 242, Exh. 3.	The noun "contact" is defined as "the coming together or touching of two objects or surfaces." 1985 American Heritage Dictionary at 315, LPL Exh. 6.	Intrinsic Evidence: '737 Patent, Figs. 1-3; Col. 1 lines 17-21, 25-29; col. 2 lines 60-66; col. 3 lines 7-10, 44-48.
Defendants' Construction			Removing selected regions only.
LPL's Support	connection between two conductors that permits a flow of current") (LPL Exh. 6).		Intrinsic Evidence: "Thereafter, as illustrated in FIG. 1d, for instance n+ amorphous silicon films 25, 26 and metal (such as Al) films 15, 16 are deposited and
LPL's Construction			The removal of selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) or other
Claim Term			selectively removing

Defendants' Support																	<u> </u>						
Defendants' Construction																							
LPL's Support	selectively etched to	form drain and source	electrodes 5, 6,	thereby completing a	thin-film transistor	unit." '737 Patent,	col. 1, lines 25-29.	"Then, as illustrated in	FIG. 2d in a sectional	view, drain and source	electrode members 15,	16 are selectively	provided, and	conducting film 30	and low-resistivity	amorphous silicon	film 20 shown in FIG.	2c are selectively	removed with said	electrode members 15,	16 serving at least as a	part of the mask to	form drain electrode 5
LPL's Construction	techniques in order to	produce a desired	pattern on the surface.				-							,									
Claim Term																							

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Defendants' Support																					
Defendants' Construction																					
LPL's Support	and source electrode 6." '737 Patent at col.	2, lines 60-66.	"[D]rain electrode 15	and source electrode	16 which doubles as a	picture cell electrode	are selectively formed	and the exposed	portion of low-	resistivity amorphous	silicon film 20 is	removed." '737	Patent at col. 3, lines	38-41.	See also '737 Patent at	col. 1, lines 14-29;	col. 2, lines 10-14, 54-	68; col. 3, lines 1-16,	24-52; Abstract; Figs.	1a-1d, 2a-2e, 3a-3d;	and claim 1.
LPL's Construction										,											
Claim Term																					

noddne	or claim ource and des least a ask"	
Defendants' Support	See support for claim term "said source and drain electrodes serving as at least a part of the mask" below.	
Defendants' Construction	At least a part of the layer which defines the edges of the selectively removed region.	
LPL's Support	"Then, as illustrated in FIG. 2d in a sectional view, drain and source electrode members 15, 16 are selectively provided, and conducting film 30 and low-resistivity amorphous silicon film 20 shown in FIG. 2c are selectively removed with said electrode members 15, 16 serving at least as a part of the mask to form drain electrode 5 and source electrode 6." '737 Patent at col. 2, lines 60-66.	See also '737 Patent at col. 1, lines 14-29; col. 2, lines 10-14, 54-68; col. 3, lines 1-16,
LPL's Construction	A "mask" is a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to material to be removed.	
Claim Term	at least a part of the mask	

Defendants' Support								Intrinsic Evidence:	[C]onducting film	30 and low-resistivity amorphous silicon
Defendants' Construction								The source and drain	electrodes make a	significant contribution to
LPL's Support	24-52; Abstract; Figs. 1a-1d, 2a-2e, 3a-3d; and claim 1; USPN 4,331,758 to Luo issued May 25, 1982	at col. 5, lines 37-col. 6, line 7 (LPL Exh. 2). Extrinsic Evidence:	1988 Penguin at 194 (defining "mask" as "A device used to	shield selected areas of a semiconductor	chip during the manufacture of semiconductor	components and	integrated circuits.) (LPL Exh. 5).	See definition of	"source electrode",	"drain electrode," and "at least a part of the
LPL's Construction								This phrase is a	combination of	previously defined constructions of
Claim Term								said source and drain	electrodes serving as	at least a part of the mask

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendants' Support
			Construction	
	"source electrode",	mask", supra.	defining the edges of	film 20 shown in FIG.
	"drain electrode," and		the selectively	2c are selectively
	"at least a part of the		removed region.	removed with said
-	mask", namely, the			[drain and source]
	source and drain			electrode members 15,
	electrodes serve as at			16 serving at least as a
	least part of the			part of the mask to
	pattern placed above a			form drain electrode 5
	surface from which			and source electrode
	material is to be			6." '737 Patent, col. 2
	selectively removed,			lines 60-66.
	where the pattern is			
	made up of material			See also '737 Patent,
	that is resistive to the			Figs. 1d, 2d, 3c; col. 4
	removal technique			lines 2-6.
	relative to material to			
	be removed.			Extrinsic Evidence:
				U.S. Patent No.
				5,905,274 to Ahn et
				al., Figs. 1E, 4E; col. 2
				lines 32-39; col. 6
				lines 55-61. Exh. 13.
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				U.S. Fatent INO.

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Defendants' Support	6,025,605 to Lyu, Figs. 2D, 3I; Col. 1 lines 60-64; col. 2 lines 49-52; col. 4	Intrinsic Evidence: '737 patent, Figs. 2a- 2e, 3a-3d; col. 1 lines 14-17, 21-31; col. 2 lines 8-35, 60-66; col. 3 lines 36-57	Extrinsic Evidence: "Form" is defined as "to give form or shape to; to give a particular shape to; to serve to make up or constitute." 1981 Webster's 447. Exh. 3.
Defendants' Construction		Giving form or shape to above and supported by or in contact with.	
LPL's Support		Intrinsic Evidence: '737 patent at col. 1, lines 14-17; col. 2, lines 8-17; Figs. 1a, 2a, 3a.	
LPL's Construction		Providing above and supported by or in contact with.	
Claim Term		"forming on"	

EXHIBIT E

EXHIBIT E

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JOINT CLAIM CONSTRUCTION STATEMENT -- EXHIBIT E U.S. Patent No. 5,825,449

"substrate" The material (such as glass) upon which a transi integrated circuit is fabricated to provide mechan support. "contact hole" An opening formed in one or more insulative lay expose a portion of a conductive layer for purpo forming an electrical connection. An opening formed in one or more insulative lay expose a portion of a conductive layer for purpo forming an electrical connection. An opening formed in one or more insulative lay expose a portion of a conductive layer for purpo forming an electrical connection. A type of display that generates an image by dir through an array of liquid crystal pixels, where to for light effused by each pixel is controlled via an field varying the orientation of the liquid crystal contained within the pixel. "material suitable for forming A transparent, electrically conductive material that a pixel electrode A pattern of transparent electrically conductive a stores charge to drive the liquid crystal material individual element of produce a pattern in the recentiques in order to produce a pattern in the recentiques in order to produce a pattern in the recentiques in order to produce a pattern in the recentiques.	CLAIM TERMS	AGREED CONSTRUCTION
play for forming	"substrate"	The material (such as glass) upon which a transistor or
play for forming		integrated circuit is fabricated to provide mechanical
play for forming		support.
play forming	"overlying"	Above.
play for forming	"contact hole"	An opening formed in one or more insulative layers to
play for forming		expose a portion of a conductive layer for purposes of
play for forming		forming an electrical connection.
play for forming	"via hole"	An opening formed in one or more insulative layers to
play for forming		expose a portion of a conductive layer for purposes of
play for forming		forming an electrical connection between two metallization
play for forming		patterns.
for forming	"liquid crystal display	A type of display that generates an image by directing light
for forming	•	through an array of liquid crystal pixels, where the amount
for forming		of light effused by each pixel is controlled via an electric
for forming		field varying the orientation of the liquid crystal molecules
for forming		contained within the pixel.
	"material suitable for forming	A transparent, electrically conductive material that can be
	a pixel electrode"	deposited and patterned, such as indium tin oxide (ITO).
	"pixel electrode	A pattern of transparent electrically conductive material that
	•	stores charge to drive the liquid crystal material within an
		individual element of the liquid crystal display device.
	"patterning"	The removal of selected portions of a surface using etching
	•	techniques in order to produce a pattern in the remaining
material.		material.

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CLAIM TERMS	AGREED CONSTRUCTION
"insulative layer" and	A thickness of non-conductive material (such as SiNx) that
"insulating film"	has high electrical resistance.
"indium tin oxide layer"	A thickness of indium tin oxide (ITO).
"semiconductor layer"	A thickness of a semiconductor material, such as amorphous
	silicon.
"impurity-doped	A thickness of semiconductor material, such as amorphous
semiconductor layer"	silicon, to which impurities (such as phosphorous atoms)
	have been added to enhance electrical conductivity.
"passivation layer"	A thickness of insulative material that provides protection
	such as electrical stability and chemical isolation.
"transparent conductive	A thickness of transparent electrically conductive material.
layer"	
conductive layer	A thickness of electrically conductive material.
one of a plurality of terminals	One of the terminals (i.e., source, drain, or gate) of a thin
of a thin film transistor	film transistor.

EXHIBIT F

EXHIBIT F

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an indium tin oxide

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

electrode 8 is deposited material." '449 Patent, "As shown in FIG. 2c, Defendant's Support a conductive layer for patterning a sputtered electrode 7 and drain layer of conductive Intrinsic Evidence: on the substrate by (emphasis added). col. 3 lines 63-66 forming source Above and supported by or in contact with. Construction Defendants' pattern on a substrate 6, 8, 10, 11 (compare '449 patent claims 1, use of "on" with use . forming a second "... forming a first LPL's Support Intrinsic Evidence: conductive layer of "overlying"). insulative layer overlying said Touching a top or side LPL believes this term has the same meaning LPL's Construction "disposed on", infra. as "formed on" and of. Claim Term

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'449 Patent, col. 4 lines surface of the substrate deposited on the entire "As shown in FIG. 2e, "As shown in FIG. 2d, 5-8 (emphasis added) a passivation layer 9, e.g., a nitride film, is by a CVD process."

"... a source electrode

substrate...." Claim

8 (emphasis added).

on said semiconductor layer . . . a passivation

Claim 10 (emphasis

source pad...."

layer overlying said

and a drain electrode

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

Defendant's Support	(ITO) layer is next	deposited on the	substrate by sputtering	or a CVD process"	'449 Patent, col. 4 lines	16-19 (emphasis	added).		See also '449 Patent,	Figs. 1-3, 5; Col. 1	lines 15-19, 34-64; col.	2 lines 5-13, 37-41, 56-	67; col. 3 lines 44-66;	col. 4 lines 39-41, 65-	68; col. 5 lines 1-17;	Claims 1, 2, 6, 8, 10,			Extrinsic Evidence:	"On" is defined as "1.a.	Used to indicate	position above and	supported by or in	contact with: The vase
Defendants' Construction									•															
LPL's Support	" patterning said	second conductive	layer to form source	electrode and a drain	electrode on said	active layer; forming a	passivation film	overlying said	substrate including	said source pad"	Claim 11 (emphasis	added).		"An amorphous	silicon active layer 4	is formed on a portion	of gate insulating film	3 overlying gate 2."	'449 patent at 1:42-44	(emphasis added.)		See also '449 patent at	1:31-48, 56-64, 2:37-	46, 3:44-62, 4:19-23,
LPL's Construction																								
Claim Term										•														

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		a sign over the door").		"Overlie" is defined as
				"to lie over or upon."
	,			The American Heritage
	•			College Dictionary 974
				(3d ed. 1997), Exh. 8;
				1995 Webster's 783, Exh. 6.
formed on	Touching a ton or side	See support for claim	Formed above and	See support for claim
		term "on" supra.	supported by or in	term "on" above.
			contact with.	
	LPL believes this term			
	has the same meaning			
	as "on", supra, and			
	"disposed on", infra.			
disposed on	Touching a top or side	See support for the	Arrange above and	See support for claim
•	of.	term "on", supra.	supported by or in	term on above.
	T.P. helieves this term			Extrinsic Evidence:
	has the same meaning			"Dispose" is defined as
	as "on" and "formed			"to arrange in a
	on" curra			particular order". 1995
	OII , supru.		·	Webster's 329, Exh. 6.
contract hole is	The contact hole is	Intrinsic Evidence:	A contact hole is made	Intrinsic Evidence:
contact note is	ITIE CUITIACE ITOIN 13	THE THOUSANT TO SECURE		

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Defendant's Support	'449 Patent, Figs. 1c-1f, 2d-2e, 3, 5 (showing contact holes made in one side and out the opposite side).	See also '449 Patent, col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38.	Extrinsic Evidence: "Through" is defined as "in one side and out the opposite or another side". 1995 Webster's 1150 (1995), Exh. 6.	See also agreed construction for "contact hole."	Intrinsic Evidence: '449 Patent, Figs. 1c-
Defendants' Construction	in one side and out the opposite side.				Made in one side and out the opposite side.
LPL's Support	Figs. 1b-1f, 2b-2e, 3-5; 1:51-2:10; 2:31-3:14; 3:50-4:41; 4:47-5:47.	("indium tin oxide layer extends through said first and second contact holes") with Figure 5 (showing	indium in oxide layer 6D entering one side of holes in insulative films 3 and 9 but not exiting out the opposite side).		See definition of "contact hole is
LPL's Construction	formed in the layer.				See definition of "contact hole is
Claim Term	provided through layer				provided through

		·	
Defendant's Support	1f, 2d-2e, 3, 5; Col. 1 lines 52-55; col. 4 lines 6-26, 47-64; col. 5 lines 8-22, 33-38.	Extrinsic Evidence: "Through" is defined as "in one side and out the opposite or another side". Webster's II New College Extrinsic Evidence 1150 (1995) ("1995 Webster's"), Exh. 6.	See also agreed construction for "contact hole."
Defendants' Construction			
LPL's Support	provided through layer", supra.		
LPL's Construction	provided through layer", supra.		
Claim Term			

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

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Defendant's Support	Intrinsic Evidence: '449 Patent, Figs. 1-5;	Extrinsic Evidence:	"Thin film technology" for circuits and systems	is defined as "a technology in which a	thin film (a few	thousand angstroms in	thickness) is applied by	vacuum deposition to an insulating	substrate". 1984 IEEE	939, Exh. 2.		Paul K. Weimer, The	TFT – A New Thin-	Film Transistor in 49	Proceedings of the IKE	1462-64 (1962). Exn.	7.
Defendants' Construction	A semiconductor device in which the	current flow between source electrode and drain electrode is	controlled by an electric field that	penetrates the semiconductor; this	field is introduced by a	gate electrode, which is	separated from the	semiconductor by an insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate.					
LPL's Support	Svidence: nt at 1:22-33;	Figs. 1-6.	prosecution history, including Amendment	of 11/17/97 at p. 5 ("The terminals of a	thin film transistor	source, and drain.")	(LPL Exh. 3). See	also Amendment of 11/17/97 at pp. 2-7.		Extrinsic Evidence:	1998 Penguin 569	("thin-film transistor	(TFT) A MOSFET	that is fabricated using	thin-film techniques	on an insulating	substrate rather than
LPL's Construction	A three terminal semiconductor device	in which the current flow through one pair of terminals, the	source and drain, is controlled or	modulated by an electric field that	penetrates the	field is introduced by	a voltage applied at	the third terminal, the	separated from the	semiconductor by an	insulating layer. The	thin-film transistor is	formed using thin-film	techniques on an	insulating substrate	rather than in a single	crystal silicon wafer.
Claim Term	thin film transistor				,												

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Defendant's Support														,						_				
Defendants' Construction																								
LPL's Support	on a semiconductor	chip.") (LPL Exh. 6);	id. at 205-207 ("field-	effect transistor (FET)	It is a three	terminal	semiconductor device	in which the current	flow through one pair	of terminals, the	source and the drain,	is controlled or	modulated by an	electric field that	penetrates the	semiconductor; this	field is introduced by	the voltage applied at	the third terminal, the	gate"); id. at 70	("chip A small	piece of single crystal	of semiconductor	material containing
LPL's Construction																					_			
Claim Term																								

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

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Claim Term	LPL's Construction	LPL's Support	Defendants' Construction	Defendant's Support
		either a single component or device or an integrated circuit.").		
selectively etching	Removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired	Intrinsic Evidence: '449 patent at 1:47-55, 2:8-10, 31-36. 50-51, 3:59-61, 3:67-4:1, 4:8- 19, 35-39, 47-50, 5:1- 15, 40-47; Figs. 1b-f, 2b-e, 3; Claims 8, 9, 11.	Having a selected portion of the substance of the first and second insulating layers removed using an etching technique.	Intrinsic Evidence: '449 Patent, Figs. 2d- 2e, 3, 5; Col. 4 lines 6- 26, 47-64; col. 5 lines 8-22, 33-38.

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JOINT CLAIM CONSTRUCTION STATEMENT – EXHIBIT F U.S. Patent No. 5,825,449

Defendant's Support	·	"Referring first to FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used
Defendants' Construction		A conductive element of a single thin-film transistor that controls the current between source and drain by a voltage applied to its terminal. The gate electrode is distinct from the gate line and the gate pad associated with the gate electrode.
LPL's Support	Extrinsic Evidence: 1998 Penguin at 190 (defining "etching" as "[c]hemical erosions of selected portions of a surface in order to produce a desired pattern on the surface.") (LPL Exh. 6). Cf. id. at 314-15 (defining "lift-off.").	Intrinsic Evidence: "[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1.
LPL's Construction	pattern on the surface.	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.
Claim Term		gate electrode

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Defendant's Support	for applying a voltage	in order to drive the	active layer in the	completed TFT	device." '449 Patent,	col. 3 lines 44-49.		See also '449 Patent,	Figs. 1-3, 5; col. 4,	lines 50-53.	-	Extrinsic Evidence:	"Gate" is defined as a	structural element of a	TFT that "controls the	current between source	and drain by a voltage	applied to its terminal".	1984 IEEE 384, Exh.	2.		"Gate" is defined as	"[a]n electrode or	electrodes in a field.
Defendants' Construction																								
LPL's Support	FIG. 2a, a conductive	layer is formed on a	transparent glass	substrate I and	patterned to form a	gate electrode 2, a	storage capacitor	electrode 2D, and a	gate pad 2C, all of the	same material. The	gate electrode is used	for applying a voltage	in order to drive the	active layer in the	completed TFT	device." '449 Patent,	3:44-49.		See also '449 patent at	1:22-38, 56-60, 2:37-	44, 2:56-61, 3:44-49,	4:47-53; 5:29-38;	Figs. 1a-f, 2a-e, 3-6;	Claims 10-11
LPL's Construction															•									
Claim Term																								

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F U.S. Patent No. 5,825,449

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Defendant's Support	effect transistor." The Penguin Dictionary of Electronics, 237 (2nd. ed. 1988) ("1988 Penguin"), Exh. 10.	Intrinsic Evidence: "Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively." '449 Patent, col. 1 lines 27- 30. "Gate pad 2B is used for receiving a voltage to drive and active
Defendants' Construction		A portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array that is necessary to communicate information from an external driving circuit to a gate electrode.
LPL's Support	·	"[A] conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate pad 2B. '449 patent at 4:65-5:1.
LPL's Construction		A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a gate driving circuit.
Claim Term		gate pad

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int's Sup		e compl	ce." '44	d. 1 line			ad wiri	ecessary	ommuni	on from	lriving c	e and so	ulating f	ely etch	urce pac	oad 2B (, '449 F	s 52-55		predeter	f passiva	d gate	; film 3 ;	y etched	
Defendant's Support		layer in the completed	TFT device." '449	Patent, col. 1 lines 34-	38.		"Since a pad wiring	layer is necessary in	order to communicate	information from an	external driving circuit	to the gate and source,	a gate insulating film 3	is selectively etched to	expose source pad 2A	and gate pad 2B (see	FIG. 1c)." '449 Patent,	col. 1 lines 52-55.		"Then, a predetermined	portion of passivation	layer 9 and gate	insulating film 3 are	selectively etched	
Defendants'	Construction									• •															
LPL's Support		material, as in the	conventional method,	and is formed at the	same time as gate 2,	storage capacitor	electrode 2D and gate	pad 2B." '449 patent	at 4:51-53.		See also '449 patent at	1:22-38, 1:52-60, 2:8-	10, 2:19-26, 3:44-49,	4:6-14, 4:21-27, 4:35-	41, 4:47-53, 4:65-5:1,	5:19-23; Figs. 1a-f, 3,	6; Claims 10-11.		Extrinsic Evidence:	1998 Penguin at 47	(defining "bonding	pads" as "[m]etal pads	arranged on a	semiconductor chip	•
LPL's Construction																									
Claim Term																									•

Defendant's Support	predetermined region of gate pad 2C. For external electrical connections It is necessary to exposed	pads 7A and 2C [sic]." '449 Patent, col. 4 lines 8-15.	See also '449 Patent, Figs. 1-3, 5; Claims 10- 11.	Extrinsic Evidence: "Gate" is defined as the structural element of a	"controls the current between source and	dram by a voltage applied to its terminal." <i>1984 IEEE</i> 384, Exh. 2.
Defendants' Construction						
LPL's Support	edge) to which wires may be bonded so that electrical connection can be made to the conponent(s) or	circuit(s) on the chip.") (LPL Exh. 6).				
LPL's Construction						
Claim Term						

					ì)						
Defendant's Support	European Patent No.	550834 to Matsuda,	Figs. 1 and 3, Col. 4	lines 14-25, Exh. 9.	See also support cited	by LPL for the term	"gad pad."	Intrinsic Evidence:	"Gate Pads 630 and	Data Pads 640 are	connected to the gate	lines and data lines to	receive datas from gate	driver and data driver	respectively." '449	Patent, Col. 1 lines 27-	30.		"Since a pad wiring	layer is necessary in	order to communicate	information from an	external driving circuit
Defendants' Construction								A portion of patterned	electrically conductive	material that is	provided near the	periphery of the thin	film transistor array	that is necessary to	communicate	information from an	external driving circuit	to a source electrode.					
LPL's Support								Intrinsic Evidence:	"[A] conductive layer	is formed on a	transparent glass	substrate 1 and	patterned to form gate	2, a storage capacitor	electrode 2D, a source	pad 2A and a gate pad	2B. '449 patent at	4:65-5:1.		"[S]ource pad 2A is	composed of gate	material, as in the	conventional method,
LPL's Construction								A portion of patterned,	electrically conductive	material that is	provided near the	periphery of the thin	film transistor array to	receive data from a	data driving circuit.		,						
Claim Term								source pad															

Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendant's Support
		and is formed at the		to the gate and source,
		same time as gate 2,	•	a gate insulating film 3
		storage capacitor		is selectively etched to
		electrode 2D and gate		expose source pad 2A
		pad 2B." '449 patent		and gate pad 2B (see
		at 4:51-53.		FIG. 1c)." '449 Patent,
				col. 1 lines 52-55.
		See also '449 patent at		
		1:8-12, 1:22-38, 1:52-		"Then, a predetermined
	-	64, 2:8-10, 2:17-22,		portion of passivation
		3:66-4:5, 4:6-14, 4:24-		layer 9 and gate
		27, 4:35-61, 4:65-5:1,		insulating film 3 are
		5:19-23, 5:48-51;		selectively etched
		Figs. 1a-f, 2d-e, 3, 6;		thereby exposing a
		Claims 10-11.		predetermined region
				of source pad 7A
		Extrinsic Evidence:		For external electrical
		1998 Penguin at 47		connections It is
		defining "bonding		necessary to exposed
		pads" as "[m]etal pads		pads 7A and 2C." '449
		arranged on a		Patent, col. 4 lines 8-
		semiconductor chip		15.
		(usually around the		
		edge) to which wires		See also '449 Patent,

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Defendant's Support	Figs. 1-3, 5; Claims 10-11.	Extrinsic Evidence:	"Source" is defined as the structural element	of a thin film transistor	that "contains the	terminal from which	charge carries flow into	channel toward the	drain. It has the	potential which is less	attractive than the drain	for the carriers in the	channel". 1984 IEEE	855, Exh. 2.	Furonean Datent No	530834 to Matsuda.	Figs. 1 and 3, Col. 4	lines 14-25, Exh 9.	700	see also support cited
Defendants' Construction																				
LPL's Support	may be bonded so that electrical connection	can be made to the component(s) or	circuit(s) on the) () () () () () () () () () (
LPL's Construction																				
Claim Term							•													

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Defendant's Support	by LPL for the term "source pad."	Intrinsic Evidence:	'449 Patent, Figs. 1b-	1f, 2b-2e, 3, 5; Col. 1	lines 39-41; col. 3 lines	50-52; col. 5 lines 1-4		Extrinsic Evidence:	"Gate" is defined as the
Defendants' Construction		A thickness of non-	conductive material	(such as SiNx) that has	high electrical	resistance and insulates	the gate electrode from	the semiconductor.	
LPL's Support		Intrinsic Evidence:	'449 patent at 1:40:44,	1:52-55, 2:11-13,	2:19-26, 2:34-36,	2:40-44, 3:50-53, 4:1-	15, 4:35-39, 4:47-50,	4:65-5:4, 5:12-15,	5:19-23, 5:40-46;
LPL's Construction		A thickness of	non-conductive	material (such as	SiNx) that has high	electrical resistance	and insulates the	transistor gate from	the semiconductor.
Claim Term		gate insulating	film						

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Defendant's Support	structural element of a	thin film transistor that	"controls the current	between source and	drain by a voltage	applied to its terminal."	1984 IEEE 384, Exh.	2.		"Insulating material" is	defined as "a substance	or body, the	conductivity or which	is zero or, in practice,	very small." 1984	<i>IEEE</i> 447, Exh. 2.		"Film" is defined as "a	thin skin or	membranous coating",	"a thin coating". 1995	Webster's 419, Exh. 6.		"Layer" is defined as a
Defendants' Construction																							-	
LPL's Support	Figs. 1b-f, 2b-e, 3, 5;	Claim 10.		Extrinsic Evidence:	1998 Penguin at 209	(defining "film" as a	"coating with a	minimal thickness	dimension.") (LPL	Exh. 6).	•	1997 American	Heritage Dictionary at	770 (defining "layer"	as a "thickness of	material covering a	surface or forming an	overlying part or	segment.") (LPL Exh.	5).				,
LPL's Construction														,										
Claim Term							·														······································			

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Defendant's Support	"thickness of material	covering a surface or	forming an overlying	part or segment."	1997 American	Heritage Dictionary	770, LPL Exh. 5.	Intrinsic Evidence:	"As shown in FIG. 1e,	the TFT is formed on	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In the	completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring
Defendants' Construction								A conductive element	of a single thin-film	transistor formed over	the source region from	which charge carriers	flow into the channel	toward the drain. The	source electrode is	distinct from the	source/data line and the	source/data pad	associated with the	source electrode.				
LPL's Support								Intrinsic Evidence:	"As shown in FIG. 1e,	the TFT is formed on	the active layer and	includes a conductive	layer deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively. Source	electrode 7 is	connected to source	pad 2A, and drain	electrode 8 is contact	with immirity-doned
LPL's Construction								A patterned,	electrically conductive	material formed over	the source region.	Current flows through	the channel between	the source electrode	and drain electrode	under control of the	gate electrode.							
Claim Term								source electrode															2 "	

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Claim Term	LPL's Construction	LPL's Support	Defendants'	Defendant's Support
			Construction	
		semiconductor layer 5		layer and drain
		and pixel electrode 6.		electrode 8, to pixel
		In the completed		electrode 6." '449
		device structure,		Patent, col. 1 line 61 –
		source electrode 7		col. 2 line 2.
		conducts a data signal,		
		received from a data		"As shown in FIG. 2c,
		wiring layer and drain		a conductive layer for
		electrode 8, to pixel		forming source
		electrode 6. The signal		electrode 7 and drain
		is stored in the form of		electrode 8 is deposited
		charge on pixel		on the substrate by
		electrode 6, thereby		patterning a sputtered
		driving the liquid		layer of conductive
		crystal." '449 patent		material. Using the
		at 1:61-2:4.		source and drain
				electrodes as masks,
		"[P]ortions of the		portions of the
		impurity-doped		impurity-doped
		semiconductor layer 5		semiconductor layer 5
		are exposed and then		are exposed and then
		etched. Source		etched. Source
		electrode 7 thus forms		electrode 7 thus forms
		part of a transistor		part of a transistor

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Defendant's Support	region and serves as	source pad 7A above	the gate insulating film	so that the same	conductive layer	constitutes part of the	source wiring and the	source electrode of the	TFT." '449 Patent,	col. 3 line $63 - \text{col. 4}$	line 5.		"Then, a conductive	layer is formed on the	substrate and etched in	accordance with a	predetermined pattern,	thereby forming a	source electrode 7 and	a drain electrode 8."	449 Patent, col. 5 lines	6-8.		See also '449 Patent,
Defendants' Construction																						·		
LPL's Support	region and serves as	source pad 7A above	the gate insulating	film so that the same	conductive layer	constitutes part of the	source wiring and the	source electrode of the	TFT." '449 patent at	3:67-4:5.		"[S]ince both the first	(45) and fourth (60)	contact holes are	formed over source	pad 2A (formed of the	same material as the	gate) and source	electrode 7,	respectively, the	source electrode 7 and	source pad 2A may be	connected to each	other in the same step
LPL's Construction													,											
Claim Term																								

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JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT F

U.S. Patent No. 5,825,449

Defendant's Support	Figs. 1e-1f, 2c-2e, 3, 5;	col. 1 lines 9-12; col. 2	lines 11-13.		Extrinsic Evidence:	"Source" is defined as	a device structure	which "contains the	terminal from which	charge carries flow into	the channel toward the	drain. It has the	potential which is less	attractive than the drain	for the carriers in the	channel." 1984 IEEE	855, Exh. 2.		"Source" is defined as	"[t]he electrode in a	field-effect transistor	that supplies charge	carriers (holes or	electrons) to the
Defendants' Construction																								
LPL's Support	that the pixel electrode	is formed. Thus, after	patterning, a first	transparent conductive	layer 6C connects	source electrode 7	with source pad 2A,	and a second	transparent conductive	layer 6 (i.e., the pixel	electrode) is	connected to drain	electrode 8." '449	patent at 4:56-64.		See also '449 patent	1:8-12, 1:22-30, 1:61-	2:4, 2:11-27, 2:37-	3:15, 3:63-4:5, 4:47-	64, 5:6-15, 5:29-39,	5:48-54; Figs. 1e-f,	2c-e, 3-6, Claims 10,	11.	
LPL's Construction																								
Claim Term																								

		j)						
Defendant's Support	interelectrode space." 1998 Penguin 532, Exh. 10.	Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on	the active layer and	includes a conductive laver deposited on the	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In the	completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring	layer and drain	electrode 8, to pixel	electrode 6." '449
Defendants' Construction		A conductive element of a single thin-film transistor formed over	the drain region into	which charge carriers flow from the source	into the channel.													•
LPL's Support		Intrinsic Evidence: "As shown in FIG. 1e, the TFT is formed on	the active layer and	includes a conductive	substrate and	simultaneously	patterned to form	source and drain	electrodes 7 and 8,	respectively In	the completed device	structure, source	electrode 7 conducts a	data signal, received	from a data wiring	layer and drain	electrode 8, to pixel	electrode 6. The
LPL's Construction		A patterned, electrically conductive material formed over	the drain region.	Current flows through	the source electrode	and drain electrode	under control of the	gate electrode.										
Claim Term		drain electrode		_			,											

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LPL's Construction
Intrinsic Evidence:
449 patent at 1:34-51
1:61-2:4, 2:11-27,
3:44-62, 4:65-5:5
5:39-47; Figs. 1b-f,
20-E, 3, 3, Ciaiiii 11
Extrinsic Evidence:
1997 American

Defendant's Support	covering a surface or forming an overlying part or segment." 1997 American Heritage Dictionary 770, LPL Exh. 5.	Intrinsic Evidence: '449 Patent, Figs. 3, 5; Col. 4 lines 47-64; col. 5 lines 8-22, 33-38. Extrinsic Evidence: "Common" is defined as "belonging to, shared by, or applying equally" 1995 Webster's 226. Exh 2.	Intrinsic Evidence: '449 Patent, Figs. 3, 5;
Defendants' Construction		A single hole.	Substantially co-axial or concentric.
LPL's Support	Heritage Dictionary at 770 (defining "layer" as a "thickness of material covering a surface or forming an overlying part or segment.") (LPL Exh. 5).	Intrinsic Evidence: '449 patent at 4:47-64; 5:8-22, 33-38; Figs. 3, 5; claim 4. Extrinsic Evidence: 1997 American Heritage Dictionary at 281 (defining "common" as "common" as "[b]elonging equally to or shared equally by two or more; joint.") (LPL Exh. 5).	Intrinsic Evidence: Substantially 449 patent at 4:47-64; or concentric.
LPL's Construction	electric field introduced by the gate electrode.	A shared hole.	Placed in line with.
Claim Term		common hole	aligned

						<u> </u>						_	′						
Defendant's Support	Col. 4 lines 47-64; col. 5 lines 8-22, 33-38.	Extrinsic Evidence: "Align" is defined as	"to place in a line." 1995 Webster's 28.	Exh. 2.	.	Intrinsic Evidence:	449 Patent, Figs. 3, 5;	Col. 4 lines 47-64; col.	5 lines 8-22, 33-38.										
Defendants' Construction						The second deposited	layer of insulating	material has a second	contact hole through it	which: (a) uncovers a	selected portion of the	second deposited	conductive layer and	(b) uncovers the region	in which the first	contact hole is located.	The first and second	contact holes must	overlan
LPL's Support	5:8-22, 33-38; Figs. 3, 5; claim 5.	Extrinsic Evidence: 1997 American	Heritage Dictionary at 34 (defining "align"	as "[t]o arrange in a line") (L.PL. Exh.	5).	Intrinsic Evidence:	'449 patent at 2:37-55;	3:2-14; 4:47-64; 5:8-	22, 33-38; Figs. 3, 5;	claims 1, 2, 5, 6, 8, 10,	and 11.								•
LPL's Construction						The second insulating	layer includes "a	second contact hole"	that exposes a portion	of the second	conductive layer. The	second insulating	layer also includes	"said first contact hole	region", i.e., it	includes part of the	first contact hole	which exposes the	predetermined portion
Claim Term						said second	insulating layer	having a second	contact hole	exposing a	predetermined	portion of said	second	conductive layer	and said first	contact hole	region		

			· .										_ '	
Defendant's Support		Intrinsic Evidence: "The TFT of the present invention	having electrical	contacts or wiring structures including	gate pad 2C, layer 6B	and layer 6A, source	pad 7A is thus	completed." '449	Patent, Col. 4 lines 24-	26; Figs. 1-5.	See also '449 Patent,	Col. 1 lines 52-55; col.	2 lines 1, 16-18; col. 4	lines 1-5.
Defendants' Construction		A structure providing an electrically conductive path that	connects at least two	terminals.										
LPL's Support		Intrinsic Evidence: '449 patent at 4:24-27.	Extrinsic Evidence:	1997 American Heritage Dictionary at	1547-1548 (defining	"wire" as "resembling	a wire, as in	slenderness") (LPL	Exh. 5).					
LPL's Construction	of the first conductive layer.	A slender structure electrically connecting at least two points.	•											
Claim Term		wiring structure									•			•

EXHIBIT L-6(c)

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Merriam Webster's

TENTH EDITION



Merriam-Webster's Collegiate® Dictionary

TENTH EDITION

Merriam-Webster, Incorporated Springfield, Massachusetts, U.S.A.



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Library of Congress Cataloging in Publication Data Main entry under title:

Merriam-Webster's collegiate dictionary. — 10th ed.

p. cm.

ISBN 0-87779-708-0 (unindexed). — ISBN 0-87779-709-9 (indexed).

— ISBN 0-87779-710-2 (deluxe). — ISBN 0-87779-707-2 (laminated cover).

1. English language—Dictionaries.

PE1628.M36 1994

423-dc20

93-32603

CIP

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works
20mnibus adj (1842) 1: of, relating to, or providing for many things at once 2: containing or including many items
om-ni-com-pe-tent \am-ni-'kam-po-tant\ adj (1827): able to handle any situation; esp: having the authority or legal capacity to act in all matters — om-ni-com-pe-tence \-tan(t)s\ n
om-ni-di-rec-tion-al \am-ni-do-'rek-shnol, -ni-, -(,)di-, -sho-n²l\ adj (1927): being in or involving all directions; esp: receiving or sending radio waves equally well in all directions (\sigma antenna anti-ous \am-ni-far-i-ous \am-ni-far-i-os, -'fer-\ adj [LL omnifarius, fr. L omni-+ -farius (as in multifarius diverse) — more at MULTIFARIOUS] (1653)
of all varieties, forms, or kinds

+ - jurius \as in manuarius diverse; — niote at mollifarious] (1653);
of all varieties, forms, or kinds
om-nif-i-cent \am-\ni-fi-s-s-nt\ adj [L omni- + E -ficent (as in magnifi-

cent)] (1677): unlimited in creative power

om-nip-o-tence \am-ni-po-ton(t)\s\ n (15c) 1: the quality or state of being omnipotent 2: an agency or force of unlimited power lom-nip-o-tent \-tont\adj [ME, fr. MF, fr. L omnipotent-, omnipotens, fr. omni-+ potent-, potens potent] (14c) 1 often cap: ALMGHTY 1 2: having virtually unlimited authority or influence 3 obs: ARRANT—

om-nip-o-tent-ly adv com-nip-otent n (1600) 1: one who is omnipotent n (2 cap: GoD 1 om-ni-pres-ence \; \(\frac{a}{a}m-ni-\) pre-z^2n(t)\s\ n (1601): the quality or state of

om-in-presente (tall-in-present substance) being omnipresent substance of the com-in-present $-z^2$ nt adj (1609): present in all places at all times om-in-range $-z^2$ nt adj (1609): present in all places at all times om-in-range $-z^2$ nt adj (1946): a system of radio navigation in which any bearing relative to a special radio transmitter on the ground may be chosen and flown by an airplane pilot — called also omnidirectional range.

omniscience \am-'ni-shən(t)s\ n [ML omniscientia, fr. L omni-+scientia knowledge — more at SCIENCE] (1612): the quality or state of

omniscient \-short\ adj [NL omniscient-, omnisciens, back-formation fr. ML omniscientia] (1604) 1: having infinite awareness, understanding, and insight 2: possessed of universal or complete knowledge — omnisciently adv

om-ni-scrently dav
om-ni-um—gath-er-um \am-nē-əm-'ga-th--rəm\ n, pl omnium—
gather-ums [L omnium (gen. pl. of omnis) + E gather + L -um, noun
ending] (1530): a miscellaneous collection (as of things or persons)
om-ni-vore \forall am-ni-vor, -vor \n [NL omnivora, neut. pl. of omnivorus,

om-nivora, heat pi. of omnivorus, fr. L (1890): one that is omnivorous
om-niv-o-rous \am-'niv-ros, -'ni-vo-\ adj [L omnivorus, fr. omni-+
-vorus -vorous] (ca. 1656) 1: feeding on both animal and vegetable
substances 2: avidly taking in everything as if devouring or consuming — om-niv-o-rous-ly ady

om-pha-los \'am(p)-fo-lâs, -los\ n [Gk, navel — more at NAVEL] (1855): a central point: HUB2, FOCAL POINT
om-pha-lo-skep-sis \, \text{im}(p)-fo-lô-'skep-sos\ n [NL, fr. Gk omphalos + skepsis examination — more at SPY] (1925): contemplation of one's navel as an aid to meditation; also: INERTIA 2

on, 'on, 'an' prep [ME an, on, prep. & adv., fr. OE; akin to OHG ana on, Gk ana up, on] (bef. 12c) 1 a — used as a function word to indicate position in contact with and supported by the top surface of (the cate position in contact with and supported by the top surface of (the book is lying ~ the table) b— used as a function word to indicate position in or in contact with an outer surface (the fly landed ~ the ceiling) (I have a cut ~ my finger) (paint ~ the wall) c— used as a function word to indicate position in close proximity with (a village ~ the sea) (stay ~ your opponent) d— used as a function word to indicate direction or location with respect to something (~ the south) (the garden is ~ the side of the house) 2 a— used as a function word to indicate a source of attachment or support (~ a string) (stand ~ one foot) (hang it ~ a nail) b— used as a function word to indicate a source of dependence (you can rely ~ me) (feeds ~ insects) (lives ~ a pension) c— used as a function word to indicate means of conveyance (~ the bus) or presence within the confines or in possession of pension c — used as a function word to indicate means of conveyance (~ the bus) or presence within the confines or in possession of (had a knife ~ him) 3 — used as a function word to indicate a time frame during which something takes place (a parade ~ Sunday) or an instant, action, or occurrence when something begins or is done (~ cue) (~ arriving home, I found your letter) (news ~ the hour) (cash ~ delivery) 4 archaic: OF 5 a — used as a function word to indicate manner of doing something; often used with the (~ the sly) (keep everything ~ the up-and-up) b — used as a function word to indicate means or agency (cut myself ~ a knife) (talk ~ the telephone) c — used as a function word to indicate a medium of expression; used orig. to refer to physical position (best show ~ television) 6 a (1)—used as a function word to indicate active involvement in a condition or status (~ fire) (~ the increase) (~ the lookout) (2): regularly using or showing the effects of using (~ drugs) b — used as a function word to indicate involvement with the activity, work, or function of (~ tour) (~ the jury) (~ duty) c — used as a function word to indicate word to indicate involvement with the activity, work, or function of (~ tour) (~ the jury) (~ duty) c—used as a function word to indicate position or status in proper relationship with a standard or objective (~ schedule) 7 a—used as a function word to indicate reason, ground, or basis (as for an action, opinion, or computation) (I have it ~ good authority) (~ one condition) (the interest will be 10 cents ~ the dollar) b—used as a function word to indicate the cause or source (profited ~ the sale of stock) c—used as a function word to indicate the focus of obligation or responsibility (drinks are ~ the house) (put the blame ~ my actions) 8 a—used as a function word to indicate the object of collision, opposition, or hostile action (bumped my head ~ a limb) (an attack ~ religion) (pulled a gun ~ me) b—used as a function word to indicate the object with respect to some disadvantage, handicap, or detriment (has three inches in height ~ me) (a 3-game lead ~ the second-place team) (the joke's ~ me) 9 a—used as a function word to indicate destination or the focus of some action, movement, or directed effort (crept up ~ him) (feast your

eyes \sim this \langle \text{working } \simeq \text{my skiing} \langle \text{made a payment } \simeq \text{the loan} \rangle \text{b} — used as a function word to indicate the focus of feelings, determination, or will (have pity \sim me) (keen \sim sports) (a curse \sim you) c—used as a function word to indicate the object with respect to some misfortune or disadvantageous event (the crops died \sim them) used as a function word to indicate the subject of study, discussion, or consideration (a book \sim insects) (reflect \sim that a moment) (agree \sim price) 10 — used as a function word to indicate reduplication or succession in a series (loss ~ loss)

20n adv (bef. 12c) 1 a: in or into a position of contact with an upper surface esp. so as to be positioned for use or operation (put the plates \sim) b: in or into a position of being attached to or covering a surface. esp: in or into the condition of being worn (put his new shoes ~) a: forward or at a more advanced point in space or time (went ~ home) (later ~) b: in continuance or succession (rambled ~) (and 3: into operation or a position permitting operation (switched the light ~>

the light \sim)
3 on adj (ca. 1541) 1: engaged in an activity or function (as a dramatic role) 2 a (1): being in operation (the radio is \sim) (2): placed so as to permit operation (the switch is \sim) b: taking place (the game is \sim) 3: aware of something — usu. used with to (my boss was \sim to me) 4: INTENDED, PLANNED (has nothing \sim for tonight) 5 Brit: talking or harping incessantly — used with about 6 chiefly Brit: regarded as possible or feasible — usu. used in negative constructions 7 a: engaged in or as if in a performance (the comedian was always ~)
b: being at a high level of performance
1-on n suffix [ISV, alter. of -one]: chemical compound not a ketone or

other oxo compound (parathion)

2-on n suffix [fr. -on (in ion)] 1: subatomic particle (nucleon) 2 a

: unit: quantum (photon) (magneton) b: basic hereditary compo-

nent (cistron) (operon)

3-on n suffix [NL, fr. -on (in argon)]: noble gas (radon)
on-again, off-again adj (1948): existing briefly and then disappear-

on-again (of-again day (14-6); existing off-again (off-again fads) on-ager (ani-jar) n [ME, wild ass, fr. L, fr. Gk onagros, fr. onos ass + agros field — more at ACRE] (14c) 1: an Asian wild ass (Equus hemionus onager syn. E. onager) that usu. has a broad dorsal stripe and is related to the kiang 2 [LL, fr. L]: a heavy catapult used in ancient and medieval times on and off adv (1855): OFF AND ON

on-and-off adj

at some indefinite time in the past: FORMERLY 4: by one degree of elationship — once and for all 1: with finality: DEFINITIVELY 2 relationship for the last time

incomplete the same time at least — at once 1: at the same time: SIMULTANEOUSLY 2: IMMEDIATELY 3: ²BOTH once adj (1691): that once was: FORMER once conj (1761): at the moment when: AS SOON AS once—over \won(t)s-\overline{0}-vor, 'won(t)s-\overline{0}, n (1914): a swift examination of survey and a swift comprehensive appraising glance.

or survey; esp: a swift comprehensive appraising glance once that conj (1874): ONCE

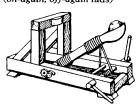
caused by a worm (*O. volvulus*) that is native to Africa but now present in parts of tropical America and is transmitted by several blackflies **on-cid-i-um** \an-'si-dē-om, aŋ-'ki-\ n [NL, fr. Gk onkos barbed hook — more at ANGLE] (ca. 1868): any of a genus (*Oncidium*) of showy tropical American chiefly epiphytic orchids **onco-** comb form [NL, fr. Gk onkos bulk, mass; akin to Gk enenkein to carry — more at ENOUGH]: tumor \(oncology \rangle
on-co-gene \(\frac{\chi_0}{\chi_0} \rangle \chi_0 \) (1969): a gene having the potential to cause a normal cell to become cancerous.

a normal cell to become cancerous on-co-gen-e-sis \angle an-e-sis \angle an-e-sis \n [NL] (ca. 1932): the induction or

formation of tumors on-co-gen-ic \-'je-nik\ adj (1936) 1: relating to tumor formation 2

tending to cause tumors on-co-ge-nic-i-ty \-j-'ni-sə-tē\ n (1944): the capacity to induce or

\ə\ abut \angle \iten, F table \ər\ further \a\ ash \a\ ace \a' mop, mar \au\out \ch\ chin \e\ bet \e\easy \g\ go \i\ hit \i\ ice \j\ job



specified by name (~ John Doe made a speech) 5: ONLY 2 (the ~

specified by name (~ John Doe made a speech) 5: ONLY 2 (the ~ person she wanted to marry)

20ne n (bef. 12c) 1— see NUMBER table 2: the number denoting unity 3 a: the first in a set or series—often used with an attributive noun (day ~) b: an article of clothing of a size designated one (wears a ~) 4: a single person or thing (has the ~ but needs the other) 5: a one-dollar bill—at one: at harmony: in a state of agreement—for one: as one example (I for one disagree)

30ne pron (13c) 1: a certain indefinitely indicated person or thing (saw ~ of his friends) 2 a: an individual of a vaguely indicated group: anyone at all (~ never knows) b— used as a third person substitute for a first person pronoun (I'd like to read more but ~ doesn't have the time) 3: a single instance of a specified action (felt like belting him ~ —John Casey)

usage Sense 2a is usu. a sign of a formal style. A formal style excludes the participation of the reader or hearer; thus one is used where a less

the participation of the reader or hearer; thus one is used where a less formal style might address the reader directly (for the consequences of such choices, one has only oneself to thank —Walker Gibson). This generic one has never been common in informal use in either British or American English, and people who start sentences with one often shift to another pronoun more natural to casual discourse (when one is learning the river, he is not allowed to do or think about anything else—Mark Twain). Use of one to replace a first-person pronoun—sense 2b—has occas, been criticized. It is more common in British English than in American (Tennetting this person of the protection of the than in American (I'm watching this pretty carefully and I hope that the issue will come up in the Lords and one may be able to speak about it —Donald Coggan, Archbishop of Canterbury).

about II —Donaid Coggan, Archoisnop of Canteroury.

one n suffix [ISV, alter. of -ene]: ketone or related or analogous compound or class of compounds (lactone) (quinone)

one another pron (1526): EACH OTHER usage see EACH OTHER

one—armed bandit \'wan-'arm(d)-\ also one—arm bandit n (1934) SLOT MACHINE 2

: SUDI MACHINE 2
one—bag-ger \ "ba-gər\ n (1952): SINGLE 2
one—di-men-sion-al adj (1883) 1: having one dimension 2: lacking depth: SUPERFICIAL (~ characters) — one—di-men-sion-al-i-ty n
one-fold \ "wən-ifold, -'fold\ adj (bef. 12c): constituting a single undi-

one-hand-ed \-han-dod\ adj (15c) 1: having or using only one hand \(\could beat \)him up \(\simes\) 2 a: designed for or requiring the use of only one hand b: effected by the use of only one hand one-horse \-hors\ adj (1750) 1: drawn or operated by one horse 2

SMALL SMALL TIME (a ~ town)

: SMALL, SMALL, SMALL, IME (a ~ town)

Onei-da \(\bar{O}\)-in-i-d>\(\chi\), pl Oneida or Oneidas [Oneida oney\(\delta\)ter.

standing rock] (1666) 1: a member of an American Indian people orig. of New York 2: the Iroquoian language of the Oneida people onei-ric \(\bar{O}\)-ini-rik\\ adj [Gk oneiros dream; akin to Arm anur\(\delta\) dream] (1859): of or relating to dreams: DREAMY — onei-ri-cal-ly \-ri-\(\delta\)-lia\(\delta\) adv k(>-)lë\ adv

onei-ro-man-cy \o-'ni-ro-man(t)-se\ n [Gk oneiros + E -mancy] (1652): divination by means of dreams one-line octave n (1931): the musical octave that begins on middle C

see PITCH illustration

as a: SINGLENESS b: INTEGRITY, WHOLENESS c: HARMONY d: SAMENESS, IDENTITY e: UNITY, UNION one-night-er\won-'ni-tar\n (ca. 1937): ONE-NIGHT STAND one-night stand n (1880) 1: a performance (as of a play or concert) given (as by a traveling group of actors or musicians) only once in each of a series of localities 2 a: a locality used for one-night stand b: a stopover for a one-night stand 3: a sexual encounter limited to a single occasion; also: a partner in such an encounter one-note \'won-'nōt\\ adj (1973): unvarying in tone or emphasis: MONOTONOUS

MONOTONOUS

one-off \won-'of\ adj (1934) Brit: limited to a single time, occasion,

or instance: ONE-SHOT, UNIQUE—one-off n

one-on-one \won-on-\won, \won-\and adj or adv (1967)

directly against a single opposing player

2: involving a direct en-

counter between one person and another

one-piece adj (1880): consisting of or made in a single undivided piece (a ~ bathing suit) — one-piecer \'wən-'pē-sər\ n

oner-ous \'ä-nə-rəs, 'ō-\ adj [ME, fr. MF onereus, fr. L onerosus, fr. oner-, onus burden; akin to Skt anas cart] (14c) 1: involving, imposing, or constituting a burden: TROUBLESOME (an ~ task) 2: having legal obligations that outweigh the advantages (~ contract) — oner-ous-ty adv — oner-ous-pieces n

ous-ly adv — oner-ous-ness n syn onerous, burdensome, oppressive, exacting mean imposing hardship. ONEROUS stresses being laborious and heavy esp. because distasteful (the onerous task of cleaning up the mess). BURDENSOME suggests causing mental as well as physical strain (burdensome responsibilities). OPPRESSIVE implies extreme harshness or severity in what is improved (the oppressive twenty of a police state). EVACTING

suggests causing mental as well as physical strain (burdensome responsibilities). OPPRESSIVE implies extreme harshness or severity in what is imposed (the oppressive tyranny of a police state). EXACTING implies rigor or sternness rather than tyranny or injustice in the demands made or in the one demanding (an exacting employer).

one-self \(\cappa_i\) won-'self, Southern also -'sef\ also one's self \(\cappa_i\) won-, wonz-\ pron (1548) 1: a person's self: one's own self — used reflexively as object of a preposition or verb or for emphasis in various constructions 2: one's normal, healthy, or sane condition or self — be oneself: to conduct oneself in a usual or fitting manner one—shot \(\fowan-\)shait\(\cappa_i\) adj (1927) 1: that is complete or effective through being done or used or applied only once \(\xi\) there is no easy \(\simpa_i\) answer to the problem\(\right) 2: that is not followed by something else of the same kind \(\alpha \simpa_i\) tax cut\(\right) — one—shot n\)
one—sid-ed \(\wan-\)'si-dad\(\alpha\) adj (1813) 1 a (1): having one side prominent: LOPSIDED (2): having or occurring on one side only b: limited to one side: PARTIAL \(\alpha \simpa_i\) interpretation\(\right) 2: UNILATERAL \(\alpha \simpa_i\) decision\(\right) — one—sid-ed-ness n\)
ones place n (1976): UNITS PLACE

one-step \'won-step\ n (1911) 1: a ballroom dance in $\frac{1}{4}$ time marked by quick walking steps backward and forward 2: music used for the one-step — one-step vi one-stop \-stap\ adj (1934): being or relating to a business that pro-

vides a complete range of goods or services of a particular kind one-tailed \'wən-'tāl(d)\ also one-tail \-'tāl\ adj (1947): being a statistical test for which the critical region consists of all values of the test statistic greater than a given value or less than a given value but not both — compare TWO-TAILED one-time \'won-'tim\ adj (1840)

1: FORMER, SOMETIME (a ~ actor)

lone-time \'wən-'tim\ adj (1840) 1: FORMER, SOMETIME \(a \sim actor\)
2: occurring only once: ONE-SHOT
2-one-time adv (1886): FORMERLY
one-to-one \, wən-tə-'wən, -də-\ adj (1873) 1: pairing each element
of a set uniquely with an element of another set 2: ONE-ON-ONE 2
one-track adj (1926): marked by often narrowly restricted attention
to or absorption in just one thing \((a \sim mind\)\)
one-two \'wən-'tii, -,tii\ n (1809) 1: a combination of two quick
blows in rapid succession in boxing; esp: a left jab followed at once by
a hard blow with the right hand 2 or one-two punch: a combination of two forces acting against something

tion of two forces acting against something

one-up \won-'pp, 'won-\ vt [back-formation fr. one-upmanship] (1963)

to practice one-upmanship on

one up adj (1919): being in a position of advantage — usu. used with

one—up-man-ship \won-'ap-man-ship\ also one—ups-man-ship\-'aps-man-\n (1952): the art or practice of outdoing or keeping one jump ahead of a friend or competitor (engaged in a round of verbal ~\circ\cone—way adj (1824) 1: that moves in or allows movement in only one direction (~ street) 2: ONE-SIDED, UNILATERAL (a ~ conversation) 3

: that functions in only one of two or more ways
on-go-ing \'on-gō-in, 'an-, -go(-)in\ adj (1877) 1 a: being actually
in process b: CONTINUING 2: continuously moving forward: GROW.

in process **b**: CONTINUING 2: continuously moving torward: GROW ING—on-go-ing-ness \-nos\ n
on-ion \'on-yon\ n [ME, fr. MF oignon, fr. L union-, unio] (14c) 1: a
widely cultivated Asian herb (Allium cepa) of the lily family with pungent edible bulbs; also: its bulb 2: any of various plants of the same
genus as the onion—on-iony \-yo-n\cdot\ adj
onion dome n (1941): a dome (as of a church) having the general
shape of an onion—onion—domed adj
onion ring n (1946): a ring of sliced onion coated with batter or
crumbs and fried

crumbs and fried

on-ion-skin $\$ -skin $\$ n (1879): a thin strong translucent paper of very

light weight oni-um \fo-ne-om\ adj [-onium] (1905): being or characterized by a usu complex cation

on-line adj or adv (1950): connected to, served by, or available through a system and esp. a computer or telecommunications system (an ~ database); also: done while connected to a system (~ computer storage)

storage)
on-look-er \'on-l\u00fc-ker, '\u00e4n-\u00e4n (1606): one that looks on; esp: a passive spectator — on-look-ing \-kin\ adj
lon-ly \'on-l\u00e4\u00e4n dj [ME, fr. OE \u00e4nlic, fr. \u00e4n one — more at ONE] (bef. 12c) 1: unquestionably the best: PEERLESS 2: alone in its class or kind: SOLE \u00e4n \u00e7 \u00e4hild\u00e4
'only adv (14c) 1 a: as a single fact or instance and nothing more of different: MERELY \u00e4hnown \u00e7 \u00e4n \u00e4 talked to her)

usage The placement of only in a sentence has been a source of studious commentary since the 18th century, most of it intended to prove by force of argument that prevailing standard usage is wrong. After 200 years of preachment the following observations may be made: the position of only in standard spoken English is not fixed, since ambiguity is avoided through sentence stress; in casual prose that keeps close to the rhythms of speech only is often placed where it would be in speech; and in edited and more formal prose only tends to be placed immediately before the word or words it modifies.

*only conj (14c) 1 a: with the restriction that: BUT (you may go, ~ come back early) b: and yet: HOWEVER (they look very nice, ~ we can't use them) 2: were it not that: EXCEPT (I'd introduce you to her, ~ you'd win her —Jack London)

*on-o-mas-tic \a-n--mas-tik\ adj [Gk onomastikos, fr. onomazein to name, fr. onoma name — more at NAME] (1716): of, relating to, or consisting of a name or names — on-o-mas-ti-cal-ly \-ti-k(a-)le\ adv

*on-o-mas-tics \-tiks\ n pl but sing or pl in constr (1930) 1 a: the science or study of the origins and forms of words esp. as used in a specialized field b: the science or study of the origin and forms of proper names of persons or places 2: the system underlying the formation and use of words esp. for proper names or of words used in a position of only in standard spoken English is not fixed, since ambigu-

mation and use of words esp. for proper names or of words used in a specialized field — on-o-mas-ti-cian \a. na-mas-ti-shan\n non-o-matol-o-gy \a. na-ma-'ta-la-j\vec{e}\n [F onomatologie, fr. Gk onomat., onoma name + F -logie -logy] (ca. 1847): ONOMASTICS — on-o-mat-la-matal-shape tables.

ma-tol-o-gist \-jist\ n

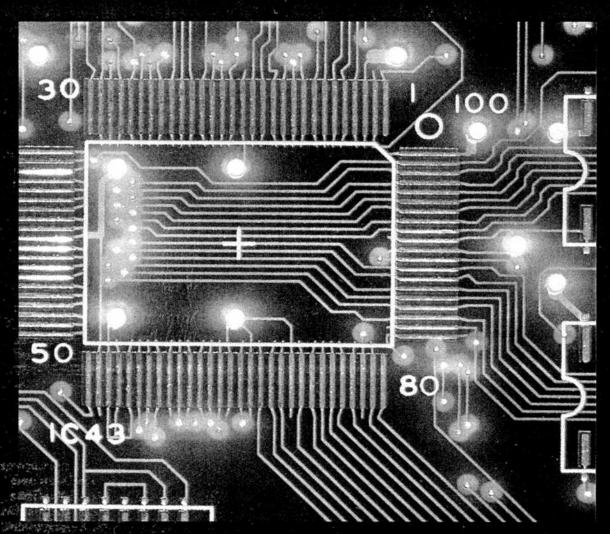
on-o-mato-poe-ia \ia-na-ima-ta-'pe-a, -ima-\ n [LL, fr. Gk onomatopoila, fr. onomat-, onoma name + poiein to make — more at POET] (ca. 1577) 1: the naming of a thing or action by a vocal imitation of the sound associated with it (as buzz, hiss) 2: the use of words whose sound suggests the sense — on-o-mato-poe-ic \-pō-ik\ or on-o-mato-poe-ic \-pō-e-tik\ adj — on-o-mato-poe-ical-ly \-'pō-o-k(a-)lē\ or on-o-mato-poe-ical-ly \-'pō-o-k(a-)lē\ on on-o-mato-poe-ical-ly \-'pō-o-k(a-)lē\ on on-o-mato-poe-ical-ly \-'pō-

poet-ic \-pō-'e-tik\ adj — on-o-mato-poe-i-cal-ly \-'pē-o-k(ə-)lē\ or on-o-mato-poe-i-cal-ly \-'pē-o-k(ə-)lē\ or On-on-da-ga \ai-nə(n)-'dō-gə, -'dā-, -'dā-\ n, pl -ga or -gas [Onondaga onotà'ke, the chief Onondaga town] (1684) 1: a member of an American Indian people of New York and Canada 2: the Iroquoian language of the Onondaga people on-ramp \'on-ramp \'on-ramp, 'ān-\ n (1958): a ramp by which one enters a limited-access highway on-rush \-,rəsh\ n (1844) 1: a rushing forward or onward 2: ONSET — on-rush-ing \-,rə-shin\ adj

EXHIBIT L-6(d)

DICTIONARY OF

EDITED BY VALERIE ILLINGWORTH





The Penguin Dictionary of ELECTRONICS

Editor: Valerie Illingworth for Market House Books

THIRD EDITION



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Published by the Penguin Group
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Penguin Putnam Inc., 375 Hudson Street, New York, New York 10014, USA
Penguin Books Australia Ltd, Ringwood, Victoria, Australia
Penguin Books Canada Ltd, 10 Alcorn Avenue, Toronto, Ontario, Canada M4V 3B2
Penguin Books (NZ) Ltd, Private Bag 102902, NSMC Auckland, New Zealand

Penguin Books Ltd, Registered Offices: Harmondsworth, Middlesex, England

First edition 1979 Second edition 1988 Third edition 1998 10 9 8 7 6 5 4 3 2

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Typeset in 8.5/10.5 pt Tmes New Roman PS Printed in England by Clays Ltd, St Ives plc

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47 bootstrapping

Boltzmann distribution law >Boltzmann constant.

bonded Denoting metal parts in a circuit that are connected together electrically so that they are at a common voltage.

bonded silvered mica capacitor > mica capacitor.

bonding pads (or bond pads) Metal pads arranged on a semiconductor chip (usually around the edge) to which wires may be bonded so that electrical connection can be made to the component(s) or circuit(s) on the chip. Bonding is usually effected by thermocompression or ultrasonic bonding. > tape automated bonding; wire bonding.

Boolean algebra An algebra introduced by George Boole in 1854 originally to provide a symbolic method for analysing human logic. Almost a century later it was also found to provide a means for analysing logical machines. An algebra is a collection of sets together with a collection of operations over those sets. A Boolean algebra may be defined as a set K of Boolean values or constants, along with a set P of three operators AND, OR, and NOT. The set K contains 2^n elements, where n is a nonzero integer, and includes two special elements denoted 0 and 1. Thus in the simplest two-valued Boolean algebra, $K = \{0,1\}$. This is the basis for all digital logic design, from the simplest logic functions to complex microprocessors and computers.

Boolean values >Boolean algebra.

booster 1. A generator or transformer inserted in a circuit in order to increase (*positive booster*) or decrease (*negative booster*) the magnitude or to change the phase of the voltage acting in the circuit. **2.** A repeater station that amplifies and retransmits a broadcast signal received from a main station, with or without a change of frequency.

bootstrapping A technique used in a variety of applications in which a capacitor – the *bootstrap capacitor* – is used to provide 100% positive > feedback for alternating currents across an amplifier stage of unity gain or less. Bootstrapping is used for control of the output signals by using the positive feedback to control the conditions in the input circuit in a desired manner.

Bootstrapping is commonly used in circuits that generate a linear timebase, particularly in a sawtooth generator. A simple sawtooth generator consists of a capacitor that is charged by means of an input load resistor and discharged by a periodic step voltage. As the capacitor is charged, the voltage increases exponentially and as the voltage increases, that across the input load (and hence the charging current) drops correspondingly. The output is approximately linear provided that only a small portion of the charging characteristic is used. The linearity may be improved by using a bootstrap circuit to maintain a constant charging current. A typical circuit is shown in Fig. a. The output is taken from an \rightarrow emitter follower, capacitively coupled via the bootstrap capacitor C_1 to the input load resistor R. As the output voltage rises, the voltage at the node between R and R_1 also rises; the voltage across R and hence the charging current is therefore maintained substantially constant.

Bootstrapping may also be used in >MOS logic circuits in order to optimize the voltage swing between the high and low logic levels. A typical bootstrapped circuit is

EXHIBIT L-6(e)

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Priority Send Enter UNITED STATES DISTRICT COURToscd CENTRAL DISTRICT OF CALIFORN \$45/JS-6. JS-2/JS-3 -

CIVIL MINUTES-GENERAL

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Case No. CV 02-6775 CBM (JTLx)

Date: October 19, 2006

Title: LG. Philips LCD Co., Ltd. v. Chunghwa Picture Tubes, Ltd., et al.

DOCKET ENTRY

ORDER CONSTRUING TERM "ONE" AS FOUND IN CLAIM ONE OF U.S. PATENT NO. 5,825,449

PRESENT:

Hon. CONSUELO B. MARSHALL, JUDGE

JOSEPH LEVARIO

Deputy Clerk

Court Reporter

ATTORNEYS PRESENT FOR PLAINTIFFS:

ATTORNEYS PRESENT FOR DEFENDANTS: N/A

N/A

PROCEEDINGS:

The matter before the Court is the parties' dispute over the proper construction over the term "one" as found in Claim 1 of U.S. Patent No. 5,825,449 (the '449 Patent).

In a bench brief filed with this Court, Defendant requests that the Court construe the language of Claim 1 of the '449 Patent as open-ended, meaning that the term "reads on products that have one or more conductive layers connected to one of a plurality of terminals of a thin film transistor." Def.'s Br. 1. The relevant claim language is:

A wiring structure comprising:

- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;
- a second conductive layer formed on a first portion of said first insulative layer;

wherein a first contact hole is provided through said first and second insulative layers . . .

and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

'449 Patent (emphasis added). Defendant seeks to have this Court interpret the last phrase beginning with "wherein one of said first and second conductive layers" Plaintiff LG.Philips argues that the phrase "one of" should be construed as "one, but not both, of the first and second conductive layers." Pl.'s Mem. 1.

Claim construction is a matter of law, and it is the duty of this Court to construe disputed

claim terms and instruct the jury as to its meaning. See Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996).

Page 3 of 3

The Federal Circuit has held that a court construing a claim must give effect to the intent of the patent applicant. See Lemelson v. General Mills, Inc., 968 F.2d 1202, 1206 (Fed. Cir. 1992). ("The prosecution history gives insight into what the applicant originally claimed as the invention, and often what the applicant gave up in order to meet the Examiner's objections."); see also Standard Oil Co. v. American Cyanamid Co., 774 F.2d 448, 452 (Fed. Cir. 1985) ("The prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance."). In the instant case, patentee LG Electronics specifically disavowed an interpretation of the claim that provided for either, or both - in other words, "one or more" - of the conductive layers being connected to a terminal of a thin film transistor; in December 1997, in order to obviate an obviousness rejection, LGE patent applicant Woo Sup Shin specifically amended the claim to articulate the "one of said first and second layers" limitation. The Court, therefore, finds that the term "one" in Claim 1 means "a single layer."

Accordingly, the Court adopts Plaintiff LG.Philips' interpretation of the relevant language in Claim 1 of the '449 Patent:

The phrase "one of" in the "wherein one of said first and second conductive layers" limitation means one, but not both, of the first and second conductive layers."

IT IS SO ORDERED.

Initials of Deputy Clerk_

cc: Judge Marshall

Parties of Record

EXHIBIT L-7

Ex. L-7 **LGD US PATENT No. 5,905,274**

INDEX OF DISPUTED TERMS

<u>Claim Terms</u>	PAGE
transistor	17
gate	17
a double layered structure	1
a second metal layer disposed on the first metal layer	1
the first metal layer including aluminum	10
the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer	10
at the sides of the aluminum first metal layer	10
the first metal layer being wider than the second metal layer by about 1 to 4 µm	1
two side portions of the first metal layer having no second layer thereon	14
two side portions of the first metal layer having no second metal layer disposed thereon	14

EXHIBIT L-7 U.S. PATENT NO. 5,905,274 TERMS IN DISPUTE

ASSERTED CLAIM 1

- L. A thin film transistor comprising:
- a substrate; and
- a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 µm.

LGD's Claim Construction

a double-layered structure¹

 a structure of an electrically conductive material that includes two sequentially deposited metal layers

a second metal layer disposed on the first metal layer² – sequentially depositing the second metal layer above and in contact with the first metal layer

the first metal layer being wider than the second metal layer by about 1 to 4 μ m³ – the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more that 1 μ m and less than 4 μ m greater than the width of the second metal layer

¹ Disputed Term "a double-layered structure" also appears in asserted claim 4 in the same context.

² Disputed Term "a second metal layer disposed on the first metal layer" also appears in asserted claim 4 in the same context.

 $^{^3}$ Disputed Term "the first metal layer being wider than the second metal layer by about 1 to 4 μ m" also appears in asserted claim 4 in the same context.

<u>INTRINSIC EVIDENCE FOR DISPUTED TERM "A DOUBLE-</u> LAYERED STRUCTURE":

A thin-film transistor includes a substrate and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 µm. A method of making such a thin film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

1:5-10

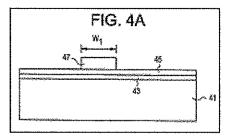
To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired

3:41-51

INTRINSIC EVIDENCE FOR DISPUTED TERM "A SECOND METAL LAYER DISPOSED ON THE FIRST METAL LAYER":

A thin-film transistor includes a substrate and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m. A method of making such a thin film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract



According to the method of labricating a thin-film transistor as described above and shown in FIGS, 1A-1F, respective first and second metal layers are formed through photolithography using different masks so as to form the gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate 21 and the substrate 11 shown in FIG. 1C, a hillock often occurs on both side portions of the first metal layer 13 which have no portion of the second metal layer 17 deposited thereon when the first metal layer 13 is wider than the second metal layer 17 as in FIG. 1C. Another problem with this related method is that the process for forming a gate is complex and requires two photoresists 15, 19 and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

2:49-65

Page 6 of 21

INTRINSIC EVIDENCE FOR DISPUTED TERM "A SECOND METAL LAYER DISPOSED ON THE FIRST METAL LAYER" (cont'd):

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

3:27-33

metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to $4 \mu m$, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic

3:46-54

A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000A and 500-2000A, respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers 43 and 45 is reduced.

5:44-54

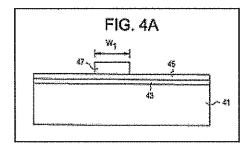
As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal

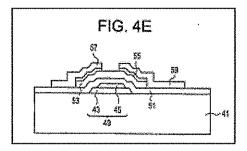
7:32-38

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING WIDER THAN THE SECOND METAL **LAYER BY ABOUT 1 TO 4 μm":**

A thin-film transistor includes a substrate and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm . A method of making such a thin film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a designated width on

Abstract





Referring to FIG. 1A, aluminum is deposited on a substrate 11 to form a first metal layer 13. A first photoresist 15 is deposited on the first metal layer 13. The first photoresist 15 is exposed and developed so as to have a certain width w1 extending along the first metal layer 13.

Referring to FIG. 1B, the first metal layer 13 is patterned via wet etching using the first photoresist 15 as a mask so that the first metal layer 13 has a certain width w1. After the first photoresist 15 is removed, a second metal layer 17 is formed by depositing Mo, Ta, or Co on the substrate 11 so as to cover the first metal layer 13. A second photoresist 19

1:51-61

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING WIDER THAN THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm" (cont'd):

Although there is no specific information available regarding a relationship of w1 to w2 of this related method, based on their understanding of this related method resulting in the structure shown in FIG. 3, the inventors of the invention described and claimed in the present application assume that the width difference w1-w2 between the first and second metal layers 13 and 17 is larger than or equal to $4 \mu m$, that is, w1-w2 $\geq 4 \mu m$.

Referring to FIG. 1D, a first insulating layer 23 is formed by depositing silicon oxide SiO₂ or silicon nitride Si₃N₄ as a single-layered or double-layered structure on the gate 21 and substrate 11. Semiconductor and ohmic contact layers

2:14-26

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer 43 is wider than the second metal layer 45 by about 1 to 4 μ m, for example, 1 μ m< μ m< μ m, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate.

4:40-52

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 µm and less than about 2 µm. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 μ m to 4.0 μ m, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal layer 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about $1 \mu m$ to $4 \mu m$.

5:21-38

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING WIDER THAN THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm" (cont'd):

neously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer 45.

Referring to FIG. 4B, the second metal layer 45 is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H₃PO₄, acetic acid CH₃COOH and nitric acid HNO₃, by means of a wet etching using the photoresist 47 as a mask. Because the portion of the second

metal layer 45 covered with the photoresist 47, as well as, exposed side portions of the second metal layer 45 are isotopically etched, the second metal layer 45 is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist 47 which is the same as the width w1 of the first metal layer 43, that is, about 1 μ m<w1-w2<4 μ m. Each side portion of the second metal layer 45 preferably has a width larger than about 0.5 μ m and less than about 2 μ m. That is, the two side portions of the

5:58-6:9

Referring to FIG. 4C, the first metal layer 43 is patterned via a wet etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist 47 as a mask. When etching the first metal layer 43 other than the portion of the layer 43 covered with the photoresist 47, the first metal layer 43 preferably has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the

6:15-24

has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers 43 and 45 also may be represented by about $1 \mu \text{m} < \text{w1} - \text{w2} < 4 \mu \text{m}$.

6:21-26

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING WIDER THAN THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm" (cont'd):

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than about 0.5 μ m, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also

6:38-46

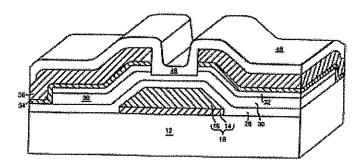
problem to be reduced. More specifically, Miyago leaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure
and then a TaOx layer is put on the Ta layer. Miyago falls to recognize the side hillock
problem with the aluminum bottom layer and also falls to recognize the necessity or
desirability for Applicant's claimed second metal layer being arranged on the first metal
layer to prevent hillock at the sides of the aluminum first metal layer and the first metal
layer being wider than the second metal layer by about 1 to 4 µm.

App. 08/918,119, 11/17/1998, Amendment.

EXTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST AYER BEING WIDER THAN THE SECOND METAL LAYER BY ABOUT 1 TO 4 μm":

It is also the Examiner's position that it is inherent that Wei teaches a first layer with a width of about 1-4 µm greater than the width of the second metal layer. See Office Action page 5, lifes 7-16. To the contrary, Wei performs an etch of the first conductor 14 until all of the exposed chromium is removed. As a result, Wei teaches etching the first conductor 14 to be the same width of the second conductor 16. Further, Wei provides no teaching or suggestion regarding the specific relationship of the widths of the first and second layers. Lastly, it is not proper to infer teachings of Wei as being inherent in a Section 103(a) rejection.

App. 09/243,556, 8/3/2001, Amendment.



GB 2253742, 09/10/1992

EXHIBIT 7 U.S. PATENT NO. 5,905,274 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A thin film transistor comprising:
- a substrate; and
- a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 µm.

LGD's Claim Construction

the first metal layer including aluminum¹ – the first metal layer containing aluminum and possibly other materials

the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer² - the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer

at the sides of the aluminum first metal layer³ - the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer

¹ Disputed Term "the first metal layer including aluminum" also appears in asserted claim 4 in the same context.

² Disputed Term "the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer" also appears in asserted claim 4 in the same context.

³Disputed Term "at the sides of the aluminum first metal layer" also appears in asserted claim 4 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER INCLUDING ALUMINUM":

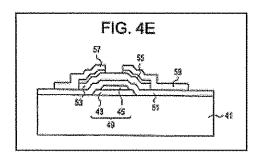
The gate 49 has a double-layered structure including the first and second metal layers 43 and 45 disposed on the substrate 41. The first metal layer 43 is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w1. The second metal layer 45 is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w2.

4:32-38

Referring to FIG. 4A, metal such as AI, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000A and 500-2000A, respectively, by means

5:42-50

INTRINSIC EVIDENCE FOR DISPUTED TERMS "THE SECOND METAL LAYER BEING ARRANGED ON THE FIRST METAL LAYER TO PREVENT HILLOCK AT THE SIDES OF THE ALUMINUM FIRST METAL LAYER" AND "AT THE SIDES OF THE ALUMINUM FIRST METAL LAYER":



To achieve the best results, the second metal layer 45 is preferably positioned substantially in the middle of the first metal layer 45, so that both side portions of the first metal layer 43 which have no portion of the second metal layer 45 disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about $0.5~\mu m$ but less than about $2~\mu m$.

The first insulating layer 51 is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate 49.

4:53-62

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 μ m and less than about 2 um. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 μ m to 4.0 μ m, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal layer 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about $1 \mu m$ to $4 \mu m$.

5:21-38

INTRINSIC EVIDENCE FOR DISPUTED TERMS "THE SECOND METAL LAYER BEING ARRANGED ON THE FIRST METAL LAYER TO PREVENT HILLOCK AT THE SIDES OF THE ALUMINUM FIRST METAL LAYER" AND "AT THE SIDES OF THE ALUMINUM FIRST METAL LAYER" (cont'd):

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon mitride Si_3N_4 on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than about 0.5 μ m, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also avoidable because a width of a portion of the first metal layer 43 which is exposed is less than about 2 μ m.

6:38-48

problem to be reduced. More specifically, Miyago teaches that in order to solve the top surface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 µm.

App. 08/918,119, 11/17/1998, Amendment.

EXHIBIT 7 U.S. PATENT NO. 5,905,274 TERMS IN DISPUTE

ASSERTED CLAIM 2

2. The thin-film transistor as claimed in claim 1, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.

ASSERTED CLAIM 5

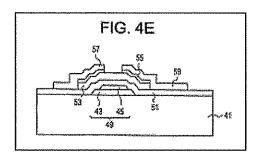
5. The thin-film transistor as claimed in claim 4, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second layer thereon have the same width as each other.

LGD's Claim Construction

two side portions of the first metal layer having no second metal layer disposed thereon — the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer

two side portions of the first metal layer having no second layer thereon — the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer

INTRINSIC EVIDENCE FOR DISPUTED TERMS "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND METAL LAYER DISPOSED THEREON " AND "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND LAYER THEREON":



To achieve the best results, the second metal layer 45 is preferably positioned substantially in the middle of the first metal layer 45, so that both side portions of the first metal layer 43 which have no portion of the second metal layer 45 disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about $0.5~\mu m$ but less than about $2~\mu m$.

The first insulating layer 51 is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate 49.

4:53-62

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 μ m and less than about 2 μ m. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 μ m to 4.0 μ m, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined

5:21-30

INTRINSIC EVIDENCE FOR DISPUTED TERMS "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND METAL LAYER DISPOSED THEREON " AND "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND LAYER THEREON " (cont'd):

The first and second metal layers 43 and 45 resulting from the single photoresist step process described above form a gate 49 having a double-layered metal structure. The gate 49 has the second metal layer 45 positioned substantially in the middle of the first metal layer 43 so that the each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than about $0.5 \, \mu \mathrm{m}$ but narrower than about 2 um. The photoresist 47 remaining on the second metal layer 45 is removed after the two etching steps are completed.

6:28-37

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of sificon oxide SiO_{π} or silicon nitride $Si_{\pi}N_{4}$ on the gate 49 and substrate 41. by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than about 0.5 um, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also

6:38-46

problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure. and then a TaOx layer is put on the Ta Isyer. Miyago fails to recognize line side hillock problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 µm.

App. 08/918,119, 11/17/1998, Amendment.

EXHIBIT 7 U.S. PATENT NO. 5,905,274 TERMS IN DISPUTE

ASSERTED CLAIM 1

1. A thin film transistor comprising:

Case 1:06-cv-00726-JJF

- a substrate; and
- a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 µm.

LGD's Claim Construction

transistor¹ – a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate

gate² – patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode

¹ Disputed Term "transistor" also appears in asserted claim 4 in the same context.

² Disputed Term "gate" also appears in asserted claim 4 in the same context.

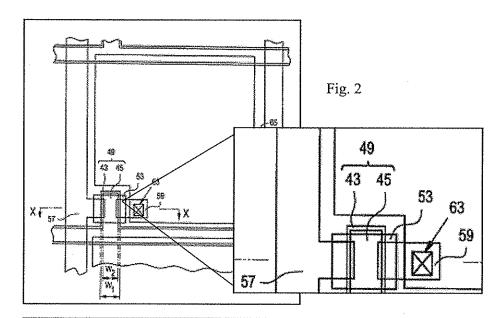
INTRINSIC EVIDENCE FOR DISPUTED TERM "TRANSISTOR":

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

1:12-16

difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and nonoverlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

1:33-39



The thin-film transistor comprises a gate 49 having a double-layered structure of a first metal layer 43, a second metal layer 45 disposed on a substrate 41, a first insulating layer 51, a second insulating layer 61, a semiconductor layer 53, an ohmic contact layer 55, a source electrode 57, a drain electrode 59, and a pixel electrode 65.

4:26-31

INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE":

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

1:9-22

EXHIBIT L-8(a)



RECEIVED

BOX AF

AUG -6 PEPLY UNDER 37 C.F.R. § 1.116 EXPEDITED PROCEDURE

TECHNOLOGY CENTER 280 EXAMINING GROUP 2823

PATENT

IN THE U.S. PATENT AND TRADEMARK OFFICE

APPLICANT:

Byung-Chul AHN et al.

CONF:

Unknown

APPL. NO.:

09/243,556

GROUP:

2823

FILED:

February 2, 1999

EXAMINER: Hawranek, S.

FOR:

THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME

AMENDMENT UNDER 37 C.F.R. § 1.116

Honorable Commissioner for Patents Washington, D.C. 20231

August 3, 2001

8p 8/31/01

Sir:

In response to the final supplemental Official Action dated July 13, 2001, please amend the above-identified application as follows. Entry of this response under Rule 116 is believed appropriate as it places the application in condition for allowance, or, in the alternative, in better form for appeal.

IN THE CLAIMS

Please amend the following claim:

(Twice Amended) A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer directly after the step of depositing the first metal layer;

forming a single photoresist having a predetermined width on the second metal layer;

patterning the second metal layer using the single photoresist as a mask; patterning the first metal layer using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm to prevent hillock at the sides of the aluminum first metal layer, thus forming a gate having a laminated structure of the first and second metal layers; and

removing the single photoresist; wherein the steps of patterning the second metal layer and the first metal layer each comprise a single step.



REMARKS

Claims 9-12, 14-19, and 37-48 are pending in the present application. Claim 9 is amended. Reconsideration of the present application is respectfully requested.

Applicants wish to thank the Examiner for the courtesy extended by the Examiner in conducting an interview regarding this application.

Prior Art Rejections

Claims 9-12 and 14-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei (GB 2 253 742 A) in view of IBM Technical Disclosure Bulletin, Vol. 35, no. 3, August, 1992, further in view of Korea (1995-4593) and further in view of Shusuke (JP 05-315615). This rejection is respectfully traversed.

It is the Examiner's position that Wei renders the use of conductive metals to form a gate stack of Al/Mo, AL/Ta or AL/Co obvious. See Office Action page 3, lines 16-19. In particular, the Examiner cited page 7, line 8+.

Contrary to the Examiners position, Wei does not render obvious "depositing a first layer on a substrate, the first metal layer including aluminum; depositing a second metal layer on the first metal layer directly after the step of depositing the first metal layer," as recited in part by claim 9.

Wei arguably teaches a semiconductor device including a gate conductor.

This gate conductor may be an <u>individual metal</u> such as titanium (Ti), chromium (Cr), tungsten (W), molybdenum (Mo), aluminum (Al) and so forth <u>or</u> may

be comprised of dual metal layers such as a first layer of titanium in contact with the substrate with a layer of molybdenum or <u>aluminum (Mo/Ti or Al/Ti, respectively) disposed therover</u> or layer of chromium disposed on a substrate with a layer of molybdenum disposed thereover (Mo/Cr).

See Wei page 7, lines 11-19.

As recited above, although Wei teaches using aluminum as a gate conductor metal, Wei teaches either a single layer gate conductor or a double layer gate conductor. In the double layer gate conductor, Wei explicitly only teaches aluminum disposed over the first layer. Based on Wei, it would not be obvious to switch the position of the layers not only because Wei provides no teaching of switching the layers, but also because one of ordinary skill in the art would not use aluminum as the first or lower layer due to the difficulties of hillock from the first layer being aluminum, which Wei does not address.

Due to Wei's lack of teachings regarding hillock, Wei also does not teach, "the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 µm to prevent hillock at the sides of the aluminum first metal layer, as recited in part by claim 9, as amended.

It is the Examiner's position that both Korean Document (1995-4593) and Shusuke (JP 05-315615) make up for the deficiencies of Wei.

KR '593 arguably teaches a semiconductor device using a double-layered metal layer as a gate, and forming an additional oxide film (aluminumtantalum oxide) through anode oxidation. KR '593 uses the additional oxide

layer to prevent hillock. Thus, even if one of ordinary skill in the art were motivated to combine the teachings of WEI and KR '593, which Applicants do not admit, KR '593 would not make up for the deficiencies of Wei because KR '593 does not teach "the first metal layer being etched to have a width greater than a width of the second metal <u>layer by about 1 to 4 µm to prevent hillock</u> at the sides of the aluminum first metal layer." Rather, KR '593 uses an additional oxidation step to prevent hillock. Thus, KR '593 does not make up for the deficiencies of Wei.

Shusuke (JP 05-315615) arguably teaches a double-layered gate semiconductor device with a aluminum layer on a substrate and a tantalum layer deposited on the aluminum layer. However, Shusuke requires at least three different etching steps to pattern the gate. As discussed in the Abstract of Shusuke, Shusuke arguably teaches dry etching the tantalum; wet etching the lower aluminum, etching the tantalum, performing a third etch of the sides of the tantalum, and additionally dry etching the upper layer of tantalum to decrease its width. Shusuke also includes an additional anode oxidation to prevent hillock of the insulating layer.

As recited in part by Claim 9, the first metal layer is "etched to have a width greater than the second metal layer by about to 4 µm to prevent hillock at the sides of the aluminum first metal layer ... and; ... the steps of patterning the second metal layer and the first metal layer each comprise a single step." Thus, due to the multitude of etching steps required by Shusuke and the only

broken of

de bregues

teaching of hillock prevention including oxidation, one of ordinary skill in the art would not be motivated to combine Shusuke and Wei to form the claimed invention. Thus, Shusuke does not make up for the deficiencies of Wei.

Additionally, even a cursory review of the IBM Technical Disclosure Bulletin ("IBM TDB") shows that this bulletin fails to make up for the deficiencies of Wei. Although the IBM TDB arguably teaches wet etching of semiconductor devices, IBM TDB does not address hillock prevention. Therefore, IBM TDB also fails to teach, the first metal layer, "etched to have a width greater than the second metal layer by about 1 to 4 µm to prevent hillock at the sides of the aluminum first metal layer," as recited in part by claim 9, as amended.

It is also the Examiner's position that it is inherent that Wei teaches a first layer with a width of about 1-4 μm greater than the width of the second See Office Action page 5, lines 7-16. To the contrary, Wei metal layer. performs an etch of the first conductor 14 until all of the exposed chromium is removed. As a result, Wei teaches etching the first conductor 14 to be the same width of the second conductor 16. Further, Wei provides no teaching or suggestion regarding the specific relationship of the widths of the first and second layers. Lastly, it is not proper to infer teachings of Wei as being inherent in a Section 103(a) rejection.

Thus, Wei does not teach, "patterning the second metal layer . . . the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μ m," as recited in part by claim 9.

Accordingly, claim 9 is allowable over the prior art. Regarding dependent claims, 10-12 and 14-19, these claims are allowable for at least the reasons of corresponding independent claim 1. Therefore, Applicants respectfully request withdrawal of this rejection.

CONCLUSION

For the foregoing reasons, Applicants respectfully request the Examiner to reconsider and withdraw all of the objections and rejections of record, and an early issuance of a Notice of Allowance is earnestly solicited.

Should there be any pending matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Jayne Saydah (Reg. No. P-48,796) at (703) 205-8000 in order to discuss these matters.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit

Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By:

Gary D. Yacura Reg. No. 35,416 P.O. Box 747

Falls Church, VA 22040-0747

(703) 205/8000

GDY/JES:ewd

Attachment

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

The claims have been amended as follows:

9. (Twice Amended) A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer directly after the step of depositing the first metal layer;

forming a single photoresist having a predetermined width on the second metal layer;

patterning the second metal layer using the single photoresist as a mask; patterning the first metal layer using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 µm to prevent hillock at the sides of the aluminum first metal layer, thus forming a gate having a laminated structure of the first and second metal layers; and

removing the single photoresist; wherein the steps of patterning the second metal layer and the first metal layer each comprise a single step.

EXHIBIT L-9

Ex. L-9 LGD US PATENT No. 6,815,321

INDEX OF DISPUTED TERMS

CLAIM TERMS	PAGE
transistor	19
Substrate	19
forming a second metal layer on the first metal layer	8
depositing a second metal layer on the first metal layer	8
a double layered metal gate	1
gategate	22
a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 µm	1
first etching layer	22
waking	25
forming a single photoresist having a predetermined width on the second metal layer	11
photoresist	11
simultaneously in a single etching step using the single photoresist as a mask	14
simultaneously patterning/patterning simultaneously	14
the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm	25
a first and a second side portion being exposed from the second metal layer	16
two side portions of the first metal layer having no second metal layer deposited thereon	16
the first metal layer including aluminum	11

EXHIBIT L-9 U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 7

7. A method of forming a thin film transistor comprising: forming a first metal layer on a substrate, forming a second metal layer on the first metal layer; simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 \(\mu\)m.

LGD's Claim Construction

a double layered metal gate — a patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μ m – the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μ m and less than 4 μ m greater than the width of the second metal layer

Page 4 of 33

INTRINSIC EVIDENCE FOR DISPUTED TERM "A DOUBLE-**LAYERED STRUCTURE":**

Document 389-19

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract

Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

1:21-27

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on

a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired

3.59-4.2

Miyago does use an aluminum layer in a double-layered gate and does

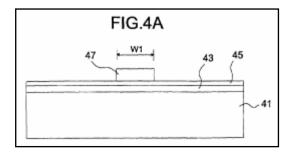
recognize a hillock problem which occurs along a top surface of a bottom aluminum layer located between the aluminum layer and a top layer. Miyago provides an entirely different solution by providing a clad structure for causing the top-surface hillock

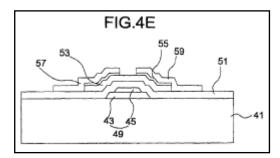
App. 08/918,119, 11/17/1998, Amendment.

INTRINSIC EVIDENCE FOR DISPUTED TERM "A TOTAL WIDTH OF THE FIRST METAL LAYER IS GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µM":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μ m. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal

Abstract





Referring to FIG. 1A, aluminum is deposited on a substrate 11 to form a first metal layer 13. A first photoresist 15 is deposited on the first metal layer 13. The first photoresist 15 is exposed and developed so as to have a certain width w1 extending along the first metal layer 13.

Referring to FIG. 1B, the first metal layer 13 is patterned via wet etching using the first photoresist 15 as a mask so that the first metal layer 13 has a certain width w1. After the first photoresist 15 is removed, a second metal layer 17 is formed by depositing Mo, Ta, or Co on the substrate 11 so as to cover the first metal layer 13. A second photoresist 19

2:1-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "A TOTAL WIDTH OF THE FIRST METAL LAYER IS GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM" (cont'd):

Although there is no specific information available regarding a relationship of w1 to w2 of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. 1C, the inventors of the invention described and claimed in the present application assume that the width difference w1-w2 between the first and second metal layers 13 and 17 is larger than or equal to $4 \mu m$, that is, w1-w2\geq 4 μm .

Referring to FIG. 1D, a first insulating layer 23 is formed by depositing silicon oxide SiO₂ or silicon nitride Si₃N₄ as a single-layered or double-layered structure on the gate 21 and substrate 11. Semiconductor and ohmic contact layers

2:32-43

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer 43 is wider than the second metal layer 45 by about 1 to 4 μ m, for example, 1 μ m<1-w2<4 μ m, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer

in such a structure having a double step difference between the substrate and the gate.

4:57-5:2

INTRINSIC EVIDENCE FOR DISPUTED TERM "A TOTAL WIDTH OF THE FIRST METAL LAYER IS GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM" (cont'd):

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 μ m and less than about 2 μ m. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 μ m to 4.0 μ m, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal layer 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about $1 \mu m$ to $4 \mu m$.

5:39-55

neously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer 45.

Referring to FIG. 4B, the second metal layer 45 is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4 , acetic acid CH_3COOH and nitric acid HNO_3 , by means of a wet etching using the photoresist 47 as a mask. Because the portion of the second metal layer 45 covered with the photoresist 47, as well as, exposed side portions of the second metal layer 45 are isotropically etched, the second metal layer 45 is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist 47 which is the same as the width w1 of the first metal layer 43, that is, about 1 μ m<w1-w2<4 μ m. Each side portion of the second metal layer 45 preferably has a width larger than about 0.5 μ m and less than about 2 μ m. That is, the two side portions of the

6:8-27

Page 8 of 33

INTRINSIC EVIDENCE FOR DISPUTED TERM "A TOTAL WIDTH OF THE FIRST METAL LAYER IS GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM " (cont'd):

Referring to FIG. 4C, the first metal layer 43 is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist 47 as a mask. When etching the first metal layer 43 other than the portion of the layer 43 covered with the photoresist 47, the first metal layer 43 preferably has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers 43 and 45 also may be represented by about 1 μ m<w1-w2<4 μ m.

6:33-44

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO₂ or silicon nitride Si₂N₄ on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than 0.5 um, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also avoidable because

6:55-63

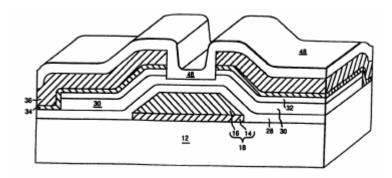
problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock. problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 μ m.

App. 08/918,119, 11/17/1998, Amendment.

INTRINSIC EVIDENCE FOR DISPUTED TERM "A TOTAL WIDTH OF THE FIRST METAL LAYER IS GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 **TO 4 μM " (cont'd):**

It is also the Examiner's position that it is inherent that Wei teaches a first layer with a width of about 1-4 µm greater than the width of the second metal layer. See Office Action page 5, lines 7-16. To the contrary, Wei performs an etch of the first conductor 14 until all of the exposed chromium is removed. As a result, Wei teaches etching the first conductor 14 to be the same width of the second conductor 16. Further, Wei provides no teaching or suggestion regarding the specific relationship of the widths of the first and second layers. Lastly, it is not proper to infer teachings of Wei as being inherent in a Section 103(a) rejection.

App. 09/243,556, 8/3/2001, Amendment.



GB 2253742, 09/10/1992

EXHIBIT U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 7

7. A method of forming a thin film transistor comprising: forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal lavers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μ m.

ASSERTED CLAIM 1

1. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 µm to about 4 µm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and removing the photoresist.

LGD's Claim Construction

forming a second metal layer on the first metal layer – sequentially depositing the second metal layer above and in contact with the first metal layer

depositing a second metal layer on the first metal layer1

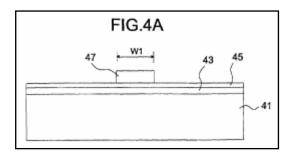
- sequentially depositing the second metal layer above and in contact with the first metal layer

¹ Disputed Term "depositing a second metal layer on the first metal layer" also appears in asserted claim 16 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERMS "FORMING A SECOND METAL LAYER ON THE FIRST METAL LAYER" AND "DEPOSITING A SECOND METAL LAYER ON THE FIRST METAL LAYER":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μ m. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract



According to the method of fabricating a thin-film transistor as described above and shown in FIGS. 1A–1F, respective first and second metal layers are formed through

photolithography using different masks so as to form the gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate 21 and the substrate 11 shown in FIG. 1C, a hillock often occurs on both side portions of the first metal layer 13 which have no portion of the second metal layer 17 deposited thereon when the first metal layer 13 is wider than the second metal layer 17 as in FIG. 1C. Another problem with this related art method is that the process for forming a gate is complex and requires two photoresists 15, 19 and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

2:65-3:14

INTRINSIC EVIDENCE FOR DISPUTED TERMS "FORMING A SECOND METAL LAYER ON THE FIRST METAL LAYER" AND "DEPOSITING A SECOND METAL LAYER ON THE FIRST METAL LAYER" (cont'd):

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

3:44-51

metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on

 \sim

a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic

3:64-4:5

Referring to FIG. 4A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500–4000 Angstroms and 500–2000 Angstroms,

respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers 43 and 45 is reduced.

5:64-6:5

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal

7:47-53

ASSERTED CLAIM 16

16. A method of waking a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μ m; and

removing the photoresist.

ASSERTED CLAIM 1

 A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 μm to about 4 μm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and removing the photoresist.

LGD's Claim Construction

the first metal layer including aluminum – the first metal layer containing aluminum and possibly other materials

forming a single photoresist having a predetermined width on the second metal layer – forming a pattern of single photosensitive material that has a specified width on the second metal layer

photoresist¹ - pattern of a
photosensitive material

¹ Disputed Term "photoresist" also appears in asserted claims 15 and 16 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER INCLUDING ALUMINUM":

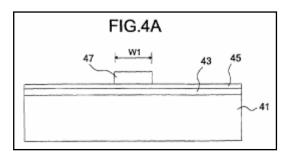
The gate 49 has a double-layered structure including the first and second metal layers 43 and 45 disposed on the substrate 41. The first metal layer 43 is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w1. The second metal layer 45 is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w2.

4:50-56

Referring to FIG. 4A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500–4000 Angstroms and 500–2000 Angstroms,

5:59-67

INTRINSIC EVIDENCE FOR DISPUTED TERMS "FORMING A SINGLE PHOTORESIST HAVING A PREDETERMINED WIDTH ON THE SECOND METAL LAYER" AND "PHOTORESIST":



Case 1:06-cv-00726-JJF

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on

a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have a desired width, thus forming a gate having a laminated structure of the first and second layers; and removing the photoresist.

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer 43 and the second metal layer 45 simultaneously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal laver 45.

metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal gate is formed. In another preferred embodiment, a single etching step is used to form the double-metal gate wherein both the first metal layer and the second metal layer are wet etched, but the difference in etching rates of the first and second metal layers produces different etching affects which result in the desired double-step structure.

3:59-4:9

6.6 - 13

7:53-61

EXHIBIT ___ U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 16

16. A method of waking a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μ m; and

removing the photoresist.

ASSERTED CLAIM 7

7. A method of forming a thin film transistor comprising: forming a first metal layer on a substrate, forming a second metal layer on the first metal layer; simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width

of the second metal layer by about 1 to 4 µm.

LGD's Claim Construction

simultaneously in a single etching step using the single photoresist as a mask – during a single etching process with a common mask

simultaneously
patterning/patterning...
simultaneously – removing
part of the first and second
metal layers during a single
etching process

INTRINSIC EVIDENCE FOR DISPUTED TERMS "SIMULTANEOUSLY IN A SINGLE ETCHING STEP USING THE SINGLE PHOTORESIST AS A MASK" AND "SIMULTANEOUSLY PATTERNING/PATTERNING...SIMULTANEOUSLY":

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer 43 and the second metal layer 45 simultaneously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer 45.

6:6-13

In still another preferred embodiment of the present invention, the gate 49 is formed through a single etching step process for etching the first and second metal layers 43 and 45 simultaneously and via a single etching step, where the second metal layer 45 is etched more quickly than the first metal layer 43 with an etching solution prepared with a mixture of phosphoric acid H₃PO₄, acetic acid CH₃COOH and nitric acid HNO₃. Because of the etching material and metals used for the first and second metal layers of the gate, only a single etching step is required. Despite the fact that

7:31-40

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal

7:47-55

EXHIBIT ___ U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 8

8. The method of claim 7, wherein the first and second metal layers are patterned so that the first metal layer has a first and a second side portion being exposed from the second metal layer, each side portion being at least about 0.5 µm in width.

ASSERTED CLAIM 22

22. The method of making a thin film transistor as claimed in claim 16, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.

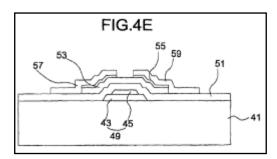
LGD's Claim Construction

a first and a second side portion being exposed from the second metal layer – first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer

two side portions of the first metal layer having no second metal layer deposited thereon

- the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A FIRST AND A SECOND SIDE PORTION BEING EXPOSED FROM THE SECOND METAL LAYER" AND "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND METAL LAYER DEPOSITED THEREON":



To achieve the best results, the second metal layer 45 is preferably positioned substantially in the middle of the first metal layer 45, so that both side portions of the first metal layer 43 which have no portion of the second metal layer 45 disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about $0.5 \mu m$ but less than about $2 \mu m$.

The first insulating layer 51 is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate 49.

5:3-13

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about $0.5~\mu m$ and less than about $2~\mu m$. Because the first metal layer 43 is wider than the second metal layer 45 by about $1.0~\mu m$ to $4.0~\mu m$, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined

5:39-48

Case 1:06-cv-00726-JJF

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A FIRST AND A SECOND SIDE PORTION BEING EXPOSED FROM THE SECOND METAL LAYER" AND "TWO SIDE PORTIONS OF THE FIRST METAL LAYER HAVING NO SECOND METAL LAYER DEPOSITED THEREON" (cont'd):

The first and second metal layers 43 and 45 resulting form the single photoresist step process described above form a gate 49 having a double-layered metal structure. The gate 49 has the second metal layer 45 positioned substantially in the middle of the first metal layer 43 so that the each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than about $0.5 \mu m$ but narrower than about 2 μm. The photoresist 47 remaining on the second metal layer 45 is removed after the two etching steps are completed.

6:45-54

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO₂ or silicon nitride Si₃N₄ on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than 0.5 um, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The

6.55-62

problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure. and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock. problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 μm .

App. 08/918,119, 11/17/1998, Amendment.

EXHIBIT ___ U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 1

 A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 μm to about 4 μm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and removing the photoresist.

LGD's Claim Construction

transistor¹ – a three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.

substrate² – the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support

¹ Disputed Term "transistor" also appears in asserted claims 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, and 22 in the same context.

² Disputed Term "substrate" also appears in asserted claims 2, 7, 16, and 17 in the same context.

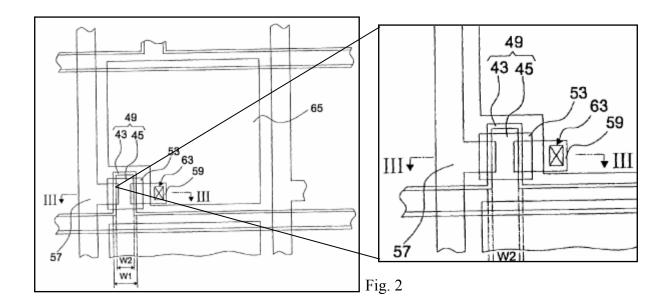
INTRINSIC EVIDENCE FOR DISPUTED TERM "TRANSISTOR":

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

1:29-33

difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and nonoverlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

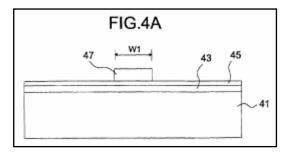
1:49-56



The thin-film transistor comprises a gate 49 having a double-layered structure of a first metal layer 43, a second metal layer 45 disposed on a substrate 41, a first insulating layer 51, a second insulating layers 61, a semiconductor layer 53, an ohmic contact layer 55, a source electrode 57, a drain electrode 59, and a pixel electrode 65.

4:44-49

INTRINSIC EVIDENCE FOR DISPUTED TERM "SUBSTRATE":



FIGS. 4A through 4F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. 4A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000 Angstroms and 500-2000 Angstroms,

5:56-67

EXHIBIT ___ U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 1

 A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 μm to about 4 μm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and removing the photoresist.

ASSERTED CLAIM 10

10. The method of claim 7, wherein the patterning step is such that the second metal layer is etched faster than the first etching layer.

LGD's Claim Construction

gate¹ – patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode

first etching layer – the first metal layer

¹ Disputed Term "gate" also appears in asserted claims 2, 7 and 17 in the same context.

INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE":

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

1:28-40

INTRINSIC EVIDENCE FOR DISPUTED TERM "FIRST ETCHING LAYER":

The gate 49 has a double-layered structure including the first and second metal layers 43 and 45 disposed on the substrate 41. The first metal layer 43 is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w1. The second metal layer 45 is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w2.

4:50-56

Referring to FIG. 4A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000 Angstroms and 500-2000 Angstroms,

5:59-67

EXHIBIT U.S. PATENT NO. 6,815,321 TERMS IN DISPUTE

ASSERTED CLAIM 16

16. A method of waking a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 µm; and

removing the photoresist.

LGD's Claim Construction

waking - making

the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to $4 \mu m$ – the first and second metal layers are etched such that the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer

INTRINSIC EVIDENCE FOR DISPUTED TERM "WAKING":

19. A method of making a thin-film transistor, comprising the step of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having a predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4µm; and

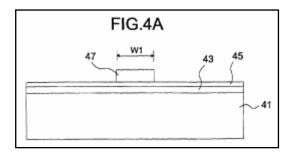
removing the photoresist.

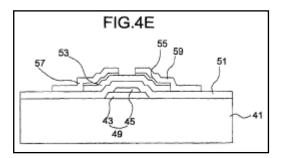
App. 10/377,732, Mar. 4, 2003, claim #16 as originally filed (renumbered at time of allowance).

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µM":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal

Abstract





Referring to FIG. 1A, aluminum is deposited on a substrate 11 to form a first metal layer 13. A first photoresist 15 is deposited on the first metal layer 13. The first photoresist 15 is exposed and developed so as to have a certain width w1 extending along the first metal layer 13.

Referring to FIG. 1B, the first metal layer 13 is patterned via wet etching using the first photoresist 15 as a mask so that the first metal layer 13 has a certain width w1. After the first photoresist 15 is removed, a second metal layer 17 is formed by depositing Mo, Ta, or Co on the substrate 11 so as to cover the first metal layer 13. A second photoresist 19

2:1-12

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM" (cont'd):

Although there is no specific information available regarding a relationship of w1 to w2 of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. 1C, the inventors of the invention described and claimed in the present application assume that the width difference w1-w2 between the first and second metal layers 13 and 17 is larger than or equal to $4 \mu m$, that is, w1-w2\geq 4 μm .

Referring to FIG. 1D, a first insulating layer 23 is formed by depositing silicon oxide SiO₂ or silicon nitride Si₃N₄ as a single-layered or double-layered structure on the gate 21 and substrate 11. Semiconductor and ohmic contact layers

2:32-43

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer 43 is wider than the second metal layer 45 by about 1 to 4 μ m, for example, 1 μ m<\text{w1}-\text{w2}<4 μ m, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer

 \sim

in such a structure having a double step difference between the substrate and the gate.

4:57-5:2

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM" (cont'd):

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 μ m and less than about 2 μ m. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 μ m to 4.0 μ m, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal layer 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about $1 \mu m$ to $4 \mu m$.

5:39-55

neously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer 45.

Referring to FIG. 4B, the second metal layer 45 is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4 , acetic acid CH_3COOH and nitric acid HNO_3 , by means of a wet etching using the photoresist 47 as a mask. Because the portion of the second metal layer 45 covered with the photoresist 47, as well as, exposed side portions of the second metal layer 45 are isotropically etched, the second metal layer 45 is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist 47 which is the same as the width w1 of the first metal layer 43, that is, about 1 μ m<w1-w2<4 μ m. Each side portion of the second metal layer 45 preferably has a width larger than about 0.5 μ m and less than about 2 μ m. That is, the two side portions of the

6:8-27

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µM" (cont'd):

Referring to FIG. 4C, the first metal layer 43 is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist 47 as a mask. When etching the first metal layer 43 other than the portion of the layer 43 covered with the photoresist 47, the first metal layer 43 preferably has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers 43 and 45 also may be represented by about 1 μ m<w1-w2<4 μ m.

6:33-44

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO₂ or silicon nitride Si₂N₄ on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than 0.5 um, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also avoidable because

6:55-63

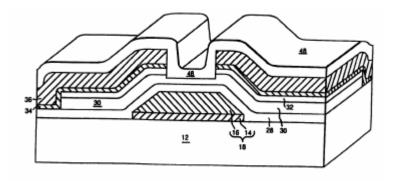
problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure. and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock. problem with the aluminum bottom layer and also fails to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 μm

App. 08/918,119, 11/17/1998, Amendment.

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST METAL LAYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µM" (cont'd):

It is also the Examiner's position that it is inherent that Wei teaches a first layer with a width of about 1-4 µm greater than the width of the second metal layer. See Office Action page 5, lines 7-16. To the contrary, Wei performs an etch of the first conductor 14 until all of the exposed chromium is removed. As a result, Wei teaches etching the first conductor 14 to be the same width of the second conductor 16. Further, Wei provides no teaching or suggestion regarding the specific relationship of the widths of the first and second layers. Lastly, it is not proper to infer teachings of Wei as being inherent in a Section 103(a) rejection.

App. 09/243,556, 8/3/2001, Amendment.



GB 2253742, 09/10/1992

EXHIBIT L-10

Ex. L-10 **LGD US PATENT No. 7,176,489**

INDEX OF DISPUTED TERMS

<u>CLAIM TERMS</u>	PAGE
transistor	15
substrate	15
a double layered metal gate	1
gategate	11
having a first metal layer and a second metal layer thereon	1
a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 µm	1
a first and second side portion being exposed from the second metal layer	11
side portion of the first metal layer	11

EXHIBIT L-10 U.S. PATENT NO. 7,176,489 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A thin film transistor comprising: a substrate; and
- a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 jim.

LGD's Claim Construction

a double layered metal gate—
a patterned structure of an
electrically conductive material
that includes two sequentially
deposited metal layers and
includes a portion that controls
current flow through the
channel between the source
electrode and drain electrode

having a first metal layer and a second metal layer thereon

- sequentially depositing the second metal layer above and in contact with the first metal layer

a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 µm – the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 µm and less than 4 µm greater than the width of the second metal layer

INTRINSIC EVIDENCE FOR DISPUTED TERM "A DOUBLE LAYERED METAL GATE":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by I to 4 µm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

1:23-28

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the

3:58-67

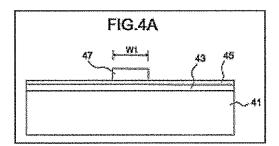
Miyago does use an aluminum layer in a double-layered gate and does recognize a hillock problem which occurs along a top surface of a bottom aluminum layer located between the aluminum layer and a top layer. Miyago provides an entirely different solution by providing a clad structure for causing the top-surface hillock

App. 08/918,119, 11/17/1998, Amendment.

INTRINSIC EVIDENCE FOR DISPUTED TERM "HAVING A FIRST METAL LAYER AND A SECOND METAL LAYER THEREON":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 µm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate. depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract



According to the method of fabricating a thin-film transistor as described above and shown in FIGS. IA-1F, respective first and second metal layers are formed through photolithography using different masks so as to form the

gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate 21 and the substrate 11 shown in FIG. 1C, a hillock often occurs on both side portions of the first metal layer 13 which have no portion of the second metal layer 17 deposited thereon when the first metal layer 13 is wider than the second metal layer 17 as in FIG. 1C. Another problem with this related art method is that the process for forming a gate is complex and requires two photoresists 15, 19 and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

2:64-3:13

INTRINSIC EVIDENCE FOR DISPUTED TERM "HAVING A FIRST METAL LAYER AND A SECOND METAL LAYER THEREON" (cont'd):

To overcome the problems discussed above, the preferred embodiments of the present invention provide a thin-film transistor which prevents a hillock and deterioration of step coverage of a later formed gate oxide layer on a double metal layer gate.

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

3:44-50

metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μ m, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the



first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic

3:63-4:4

Referring to FIG. 4A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000 Angstroms and 500-2000 Angstroms.



respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers 43 and 45 is reduced.

5:61-6:5

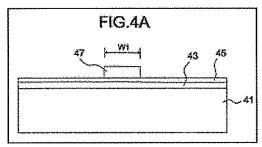
INTRINSIC EVIDENCE FOR DISPUTED TERM "HAVING A FIRST METAL LAYER AND A SECOND METAL LAYER THEREON" (cont'd):

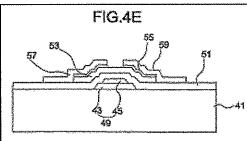
As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal 8:6-12

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A TOTAL WIDTH OF THE FIRST METAL LAYER BEING GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm":

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 µm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

Abstract





Referring to FIG. 1A, aluminum is deposited on a substrate 11 to form a first metal layer 13. A first photoresist 15 is deposited on the first metal layer 13. The first photoresist 15 is exposed and developed so as to have a certain width w1 extending along the first metal layer 13.

Referring to FIG. 1B, the first metal layer 13 is patterned via wet etching using the first photoresist 15 as a mask so that the first metal layer 13 has a certain width w1. After the first photoresist 15 is removed, a second metal layer 17 is formed by depositing Mo, Ta, or Co on the substrate 11 so as to cover the first metal layer 13. A second photoresist 19

2:1-11

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A TOTAL WIDTH OF THE FIRST METAL LAYER BEING GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μm" (cont'd):

In the gate 21, shown in FIG. 1C, the second metal layer 17 is preferably centrally located on the first metal layer 13. Although there is no specific information available regarding a relationship of w1 to w2 of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. 1C, the inventors of the invention described and claimed in the present application assume that the width difference w1-w2 between the first and second metal layers 13 and 17 is larger than or equal to 4 µm, that is, w1-w2 ≥ 4 µm.

Referring to FIG. 1D, a first insulating layer 23 is formed by depositing silicon oxide SiO₂ or silicon nitride Si₃N₄ as a single-layered or double-layered structure on the gate 21 and substrate 11. Semiconductor and ohmic contact layers

2:31-42

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer 43 is wider than the second metal layer 45 by about 1 to 4 µm, for example, 1 µm<w1-w2<4 µm, provides maximum prevention of determined of determined that a structure wherein the first metal layer 43 is wider than the second metal layer 45 by about 1 to 4 µm, for example, 1



rioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate.

4:58-5:3

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INTRINSIC EVIDENCE FOR DISPUTED TERMS "A TOTAL WIDTH OF THE FIRST METAL LAYER BEING GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm" (cont'd):

neously. In the single photoresist step, a photoresist 47 is deposited on the second metal layer 45 and then the photoresist 47 is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer 45.

Referring to FIG. 4B, the second metal layer 45 is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H₂PO₄, acetic acid CH₂COOH and nitric acid HNO3, by means of a wet etching using the photoresist 47 as a mask. Because the portion of the second metal layer 45 covered with the photoresist 47, as well as, exposed side portions of the second metal layer 45 are isotropically etched, the second metal layer 45 is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist 47 which is the same as the width w1 of the first metal layer 43, that is, about 1 jun<w1-w2<4 jun. Each side portion of the second metal layer 45 preferably has a width larger than about 0.5 µm and less than about 2 µm. That is, the two side portions of the

6:9-27

Referring to FIG. 4C, the first metal layer 43 is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist 47 as a mask. When etching the first metal layer 43 other than the portion of the layer 43 covered with the photoresist 47, the first metal layer 43 preferably has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the

6:33-42

has the same width w1 of the photoresist 47. Thus, patterning of the first and second metal layers 43, 45, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers 43 and 45 also may be represented by about 1 µm<w1-w2<4 um.

6:39-44

Page 11 of 19

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A TOTAL WIDTH OF THE FIRST METAL LAYER BEING GREATER THAN A TOTAL WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 µm" (cont'd):

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO₂ or silicon nitride Si₂N₄ on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than 0.5 um, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also avoidable because

6:55-63

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 µm and less than about 2 µm. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 jun to 4.0 jun. double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal layer 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about $1 \mu m$ to $4 \mu m$.

5:39-55

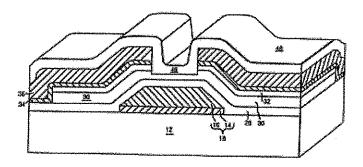
problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillook problem, a first tantalum layer is put on the Al-Mo double layer structure and then a TaO≍ layer is put on the Ta layer. Miyago falls to recognize the side hillock problem with the aluminum bottom layer and also falls to recognize the necessity or desirability for Applicant's claimed second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer and the first metal layer being wider than the second metal layer by about 1 to 4 µm.

App. 08/918,119, 11/17/1998, Amendment.

INTRINSIC EVIDENCE FOR DISPUTED TERM "THE FIRST AYER BEING ETCHED TO HAVE A WIDTH GREATER THAN A WIDTH OF THE SECOND METAL LAYER BY ABOUT 1 TO 4 μM" (cont'd):

It is also the Examiner's position that it is inherent that Wei teaches a first layer with a width of about 1-4 µm greater than the width of the second metal layer. See Office Action page 5, liftes 7-16. To the contrary, Wei performs an etch of the first conductor 14 until all of the exposed chromium is removed. As a result, Wei teaches etching the first conductor 14 to be the same width of the second conductor 16. Further, Wei provides no teaching or suggestion regarding the specific relationship of the widths of the first and second layers. Lastly, it is not proper to infer teachings of Wei as being inherent in a Section 103(a) rejection.

App. 09/243,556, 8/3/2001, Amendment.



GB 2253742, 09/10/1992

EXHIBIT H U.S. PATENT NO. 7,176,489 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A thin film transistor comprising:
- a substrate; and
- a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal layer being greater than a total width of the second metal layer by about I to 4 µm.

ASSERTED CLAIM 2

2. The transistor of claim 1, wherein the first metal layer has a first and second side portion being exposed from the second metal layer, each side portion being at least about 0.5 um in width.

ASSERTED CLAIM 3

3. The transistor of claim 2, wherein each side portion of the first metal layer is less than about 2 µm in width.

LGD's Claim Construction

gate – patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode

a first and second side portion being exposed from the second metal layer - first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer

side portion of the first metal layer - side surface of the first metal layer exposed to the subsequently deposited gate insulating layer

INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE":

2. Discussion of Related Art

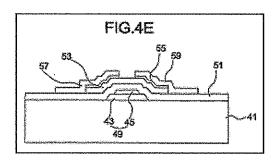
An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

1:23-40

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A FIRST AND SECOND SIDE PORTION BEING EXPOSED FROM THE SECOND METAL LAYER" AND "SIDE PORTION OF THE FIRST METAL LAYER":



Case 1:06-cv-00726-JJF

To achieve the best results, the second metal layer 45 is preferably positioned substantially in the middle of the first metal layer 45, so that both side portions of the first metal layer 43 which have no portion of the second metal layer 45 disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about 0.5 µm but less than about 2 µm.

The first insulating layer 51 is preferably formed by depositing single layer of silicon oxide SiO, or silicon nitride Si_3N_4 on the substrate including the gate 49.

5:4-13

In the first and second metal layers 43 and 45 constituting the gate 49, each side portion of the first metal layer 43 having no portion of the second metal layer 45 thereon has a width that is preferably larger than about 0.5 µm and less than about 2 µm. Because the first metal layer 43 is wider than the second metal layer 45 by about 1.0 µm to 4.0 µm, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate 49 and substrate 41. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer 51 which deterioration occurs in prior art devices. The hillock in the first metal faver 43 is also avoidable because the width difference between the first and second metal layers 43 and 45 is between about 1 μm to 4 μm.

5:39-55

INTRINSIC EVIDENCE FOR DISPUTED TERMS "A FIRST AND SECOND SIDE PORTION BEING EXPOSED FROM THE SECOND METAL LAYER" AND "SIDE PORTION OF THE FIRST METAL LAYER" (cont'd):

Referring to FIG. 4D, a first insulating layer 51 is formed by depositing a single layer or double layers of silicon oxide SiO₂ or silicon nitride Si₃N₄ on the gate 49 and substrate 41 by CVD. Because each side portion of the first metal layer 43 having no second metal layer 45 thereon is wider than 0.5 μm, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer 51 from being deteriorated as in prior art devices. The hillock in the first metal layer 43 is also avoidable because a width of a portion of the first metal layer 43 which is exposed is less than about 2 μm.

6:55-65

problem to be reduced. More specifically, Miyago teaches that in order to solve the topsurface hillock problem, a first tantalum layer is put on the Al-Mo double layer structure
and then a TaOx layer is put on the Ta layer. Miyago fails to recognize the side hillock
problem with the aluminum bottom layer and also fails to recognize the necessity or
desirability for Applicant's claimed second metal layer being arranged on the first metal
layer to prevent hillock at the sides of the aluminum first metal layer and the first metal
layer being wider than the second metal layer by about 1 to 4 µm.

Appl. No. 08/918,119, 11/17/1998 Amendment

EXHIBIT H U.S. PATENT NO. 7,176,489 TERMS IN DISPUTE

ASSERTED CLAIM 1

- 1. A thin film transistor comprising:
- a substrate, and
- a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 um.

LGD's Claim Construction

 $transistor^1 - a three-terminal$ semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by the insulating layer. The thin-film transistor is formed using thinfilm techniques on an insulating substrate rather than a single crystal silicon wafer.

substrate - the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support

¹ Disputed Term "transistor" also appears in asserted claims 2 and 3 in the same context.

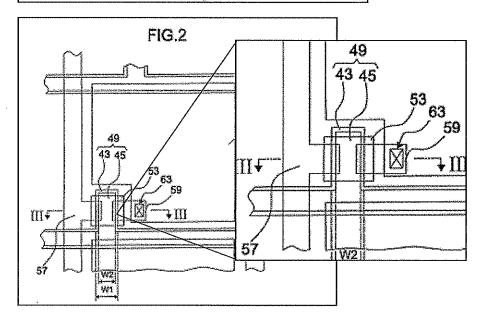
INTRINSIC EVIDENCE FOR DISPUTED TERM "TRANSISTOR":

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electredes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

1:30-34

difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and nonoverlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

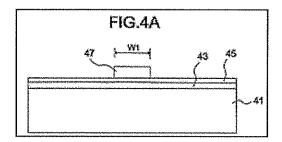
1:50-56



The thin-film transistor comprises a gate 49 having a double-layered structure of a first metal layer 43, a second metal layer 45 disposed on a substrate 41, a first insulating layer 51, a second insulating layers 61, a semiconductor layer 53, an ohmic contact layer 55, a source electrode 57. a drain electrode 59, and a pixel electrode 65.

4:44-49

INTRINSIC EVIDENCE FOR DISPUTED TERM "SUBSTRATE":



FIGS. 4A through 4F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. 4A, metal such as Al. Cu, or Au is deposited on a substrate so as to form a first metal layer 43. A second metal layer 45 is formed from Mo, Ta, or Co and deposited on the first metal layer 43 without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers 43 and 45 are sequentially deposited so as to preferably have a thickness as large as about 500-4000 Angstroms and 500-2000 Angstroms,

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